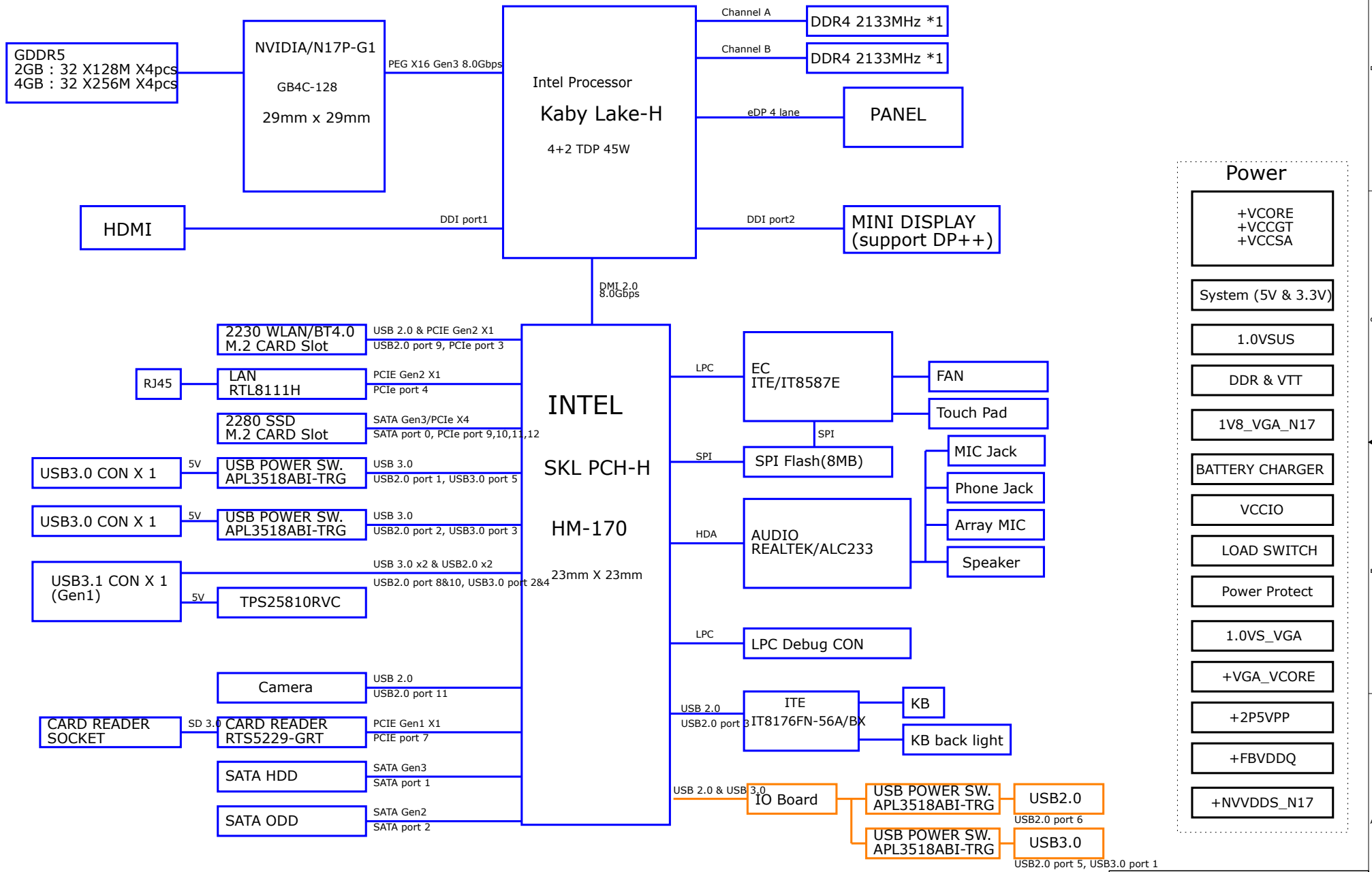
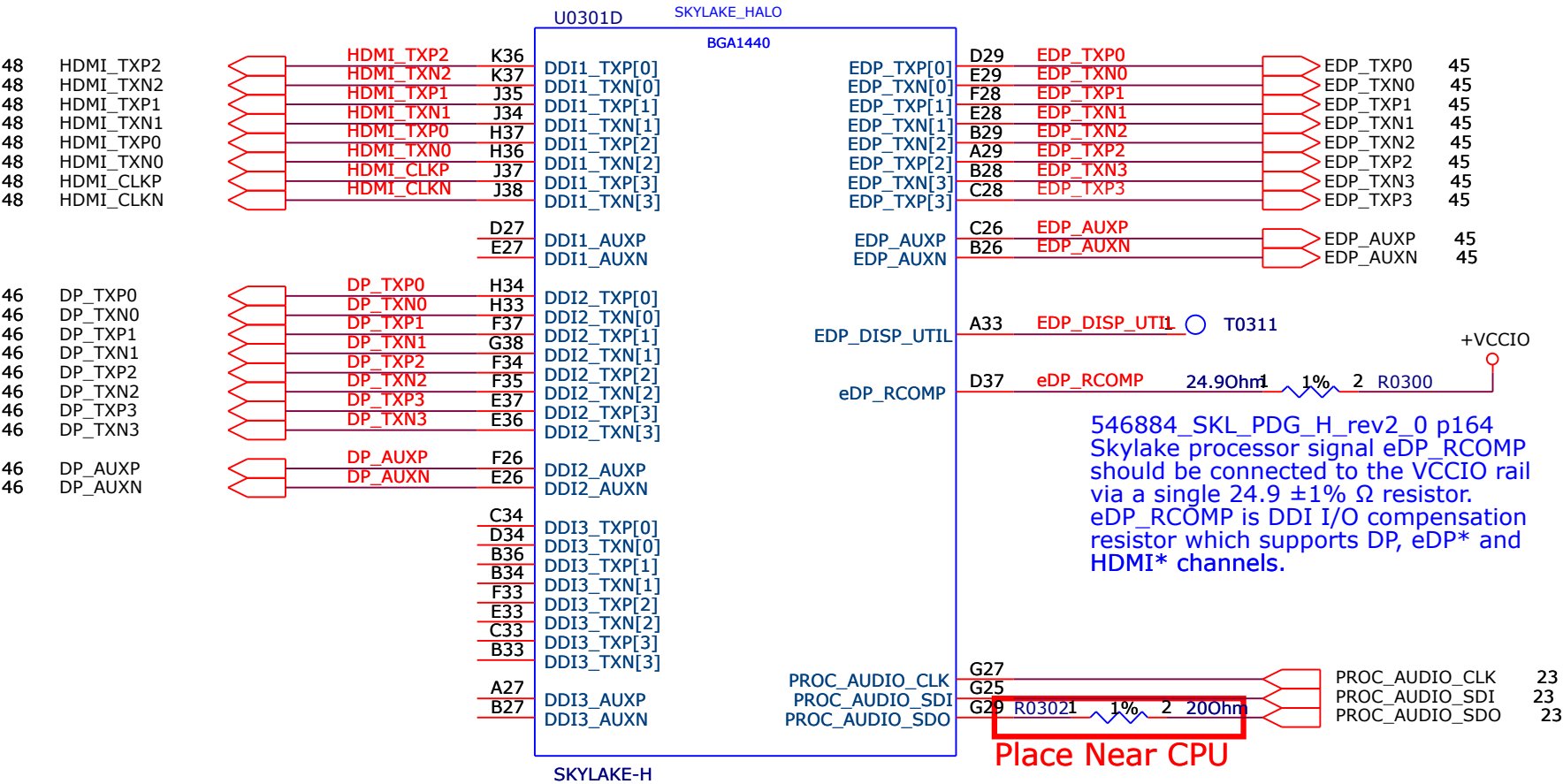


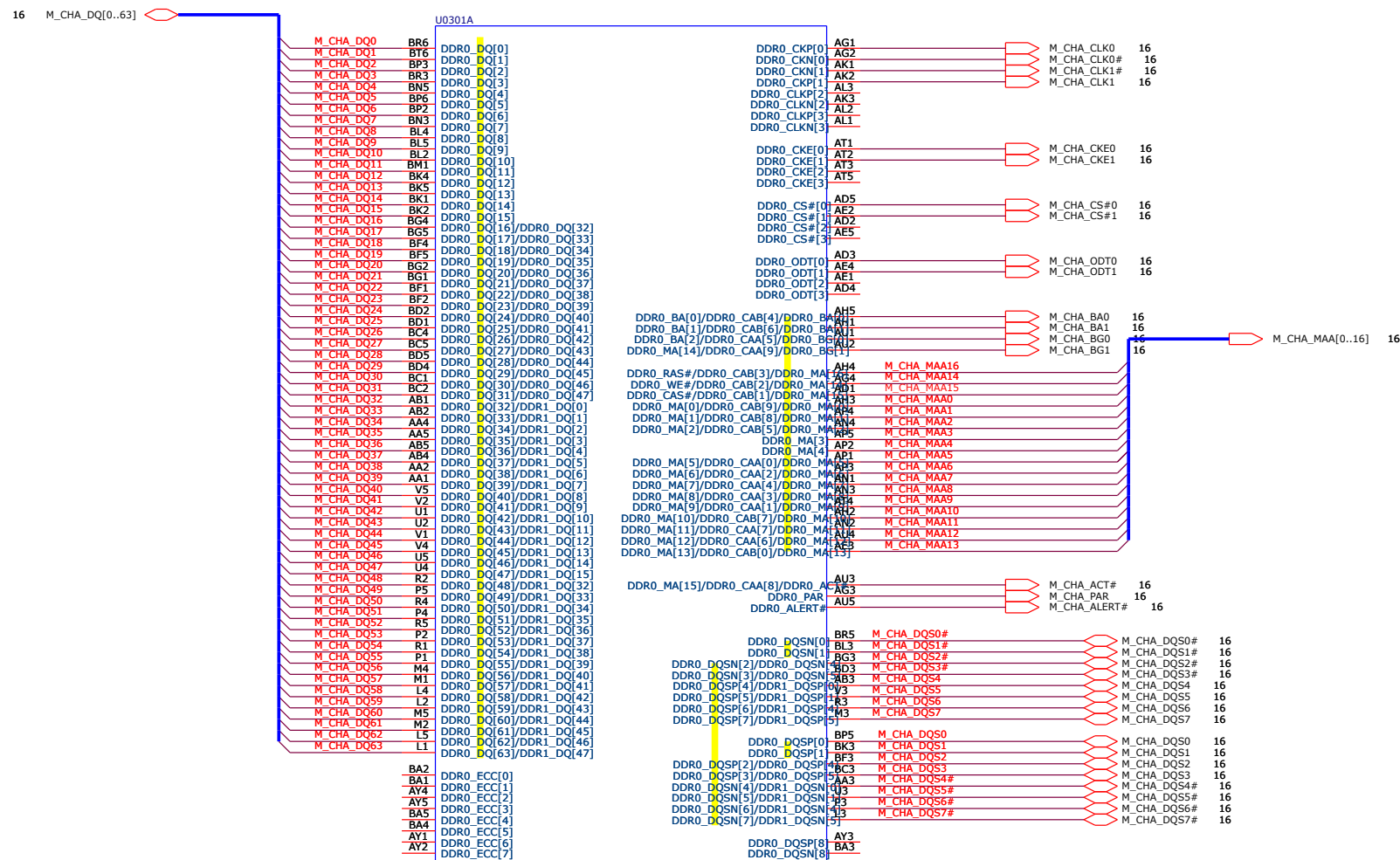
# GL753 Block Diagram



# 3.CPU\_DDI/EDP



# 04.CPU DDR4 Channel0



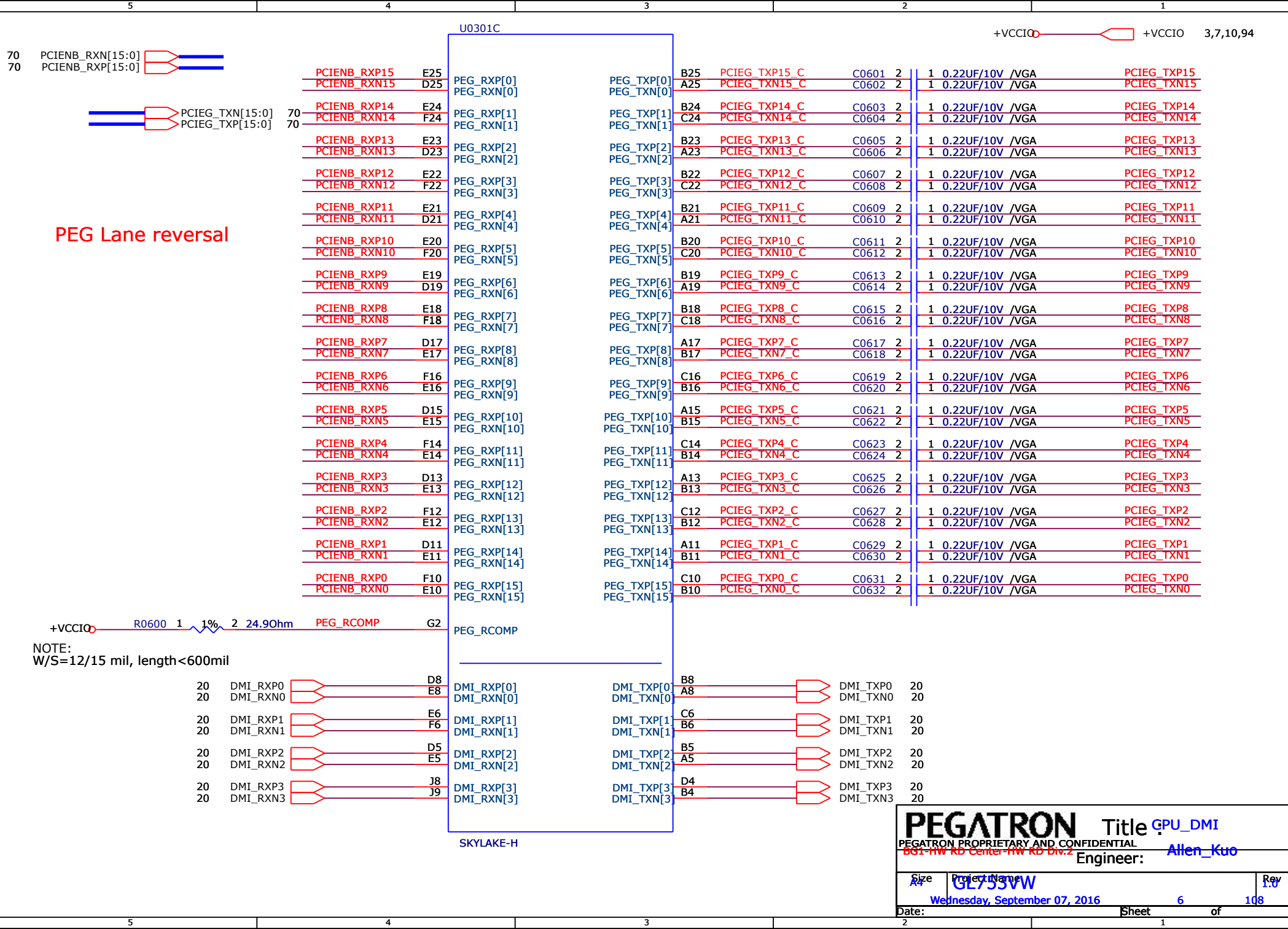
PEGATRON DT-MB RESTRICTED SECRET

<b>PEGATRON</b>		Title CPU_DDR4_A	
PEGATRON PROPRIETARY AND CONFIDENTIAL		Engineer: Allen_Kuo	
Size A3	Project Name GL753VW	Date: Wednesday, September 07, 2016	Rev 1.08
Date:		Sheet 4	of 108

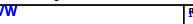
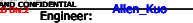
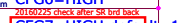
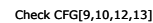
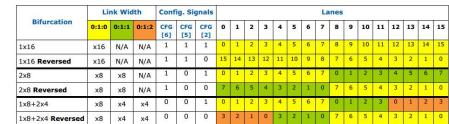
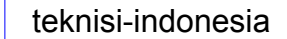
**A**



<b>PEGATRON</b>		Title: <b>CPU_DDR4_B</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
DCL-TWR RD Center-TWR RD Div-2			
Engineer:		<b>Allen_Kuo</b>	
Size	Project Name		Rev
<b>Custom</b>	<b>GL753VW</b>		
<b>Wednesday, September 07, 2016</b>		<b>5</b>	<b>108</b>
Date:	Sheet	of	

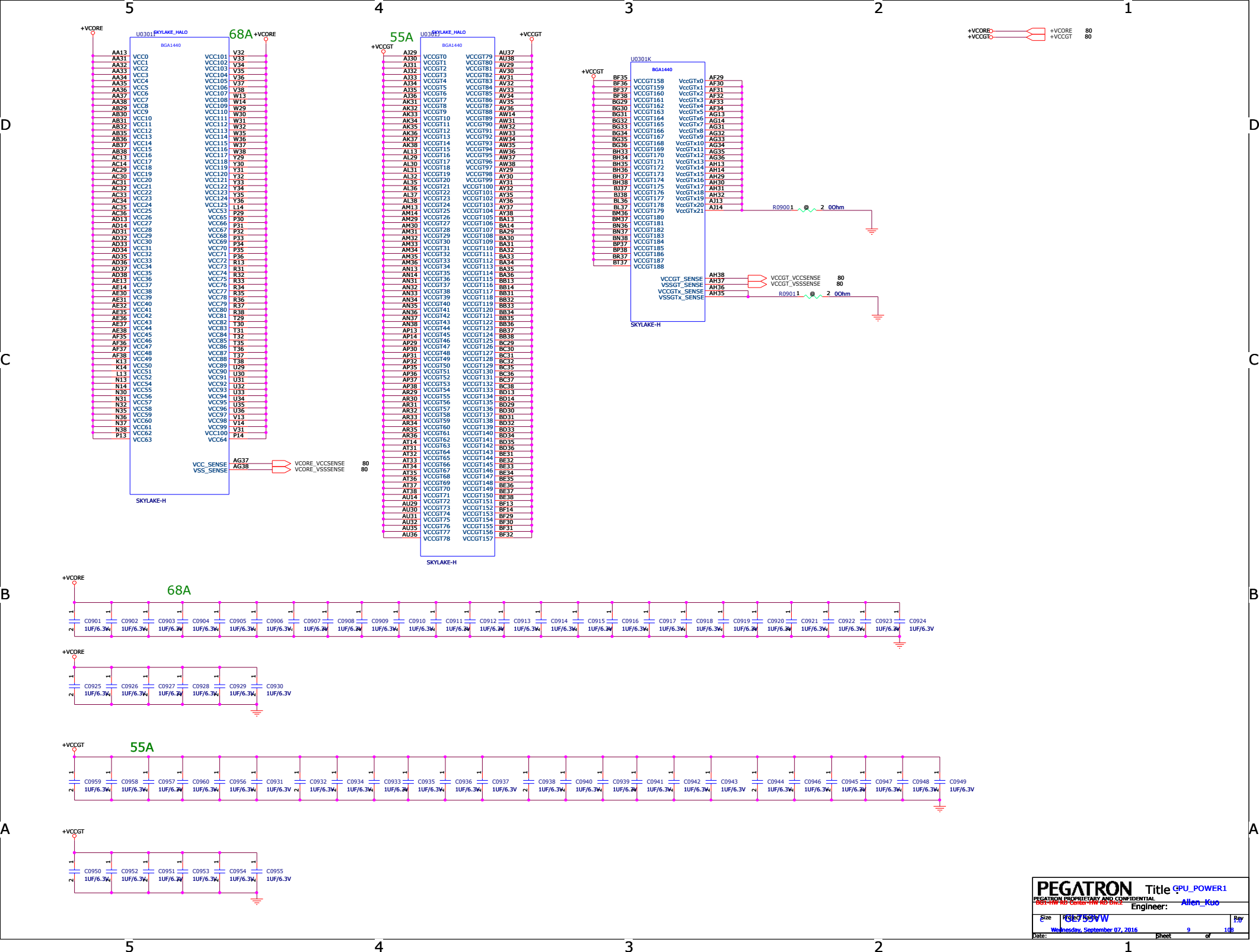


Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2-W3-W4-W5 [inches]	W51 [inches]	W52 [inches]	R <sub>01</sub> [Ω]	R <sub>02</sub> [Ω]	R <sub>03</sub> [Ω]	R <sub>04</sub> [Ω]	VCC [V]
VIDSOUT							100	100	0	10	
VIDSOK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.6
VIDALERT #							56	Empty	220	0	











546884\_SKL\_PDG\_H\_rev2\_0 (p.622)  
 Skylake processor will internally power gate the VDDQ rail, system context is in suspended-to-RAM state, and SKL PCH-LP placed in Deep Sx state. Therefore, unlike previous platform, there is no need to externally gate the VDDQ rail of the Processor.

Seq15. VCCSA

Seq13. VDDQ

Seq14. VccIO

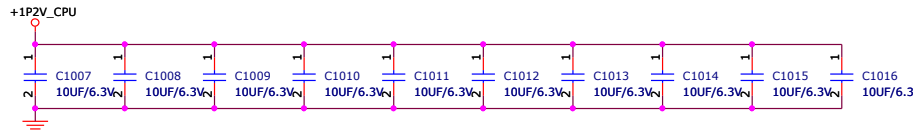
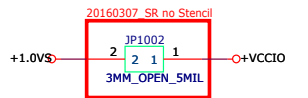
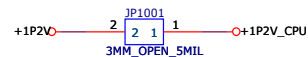
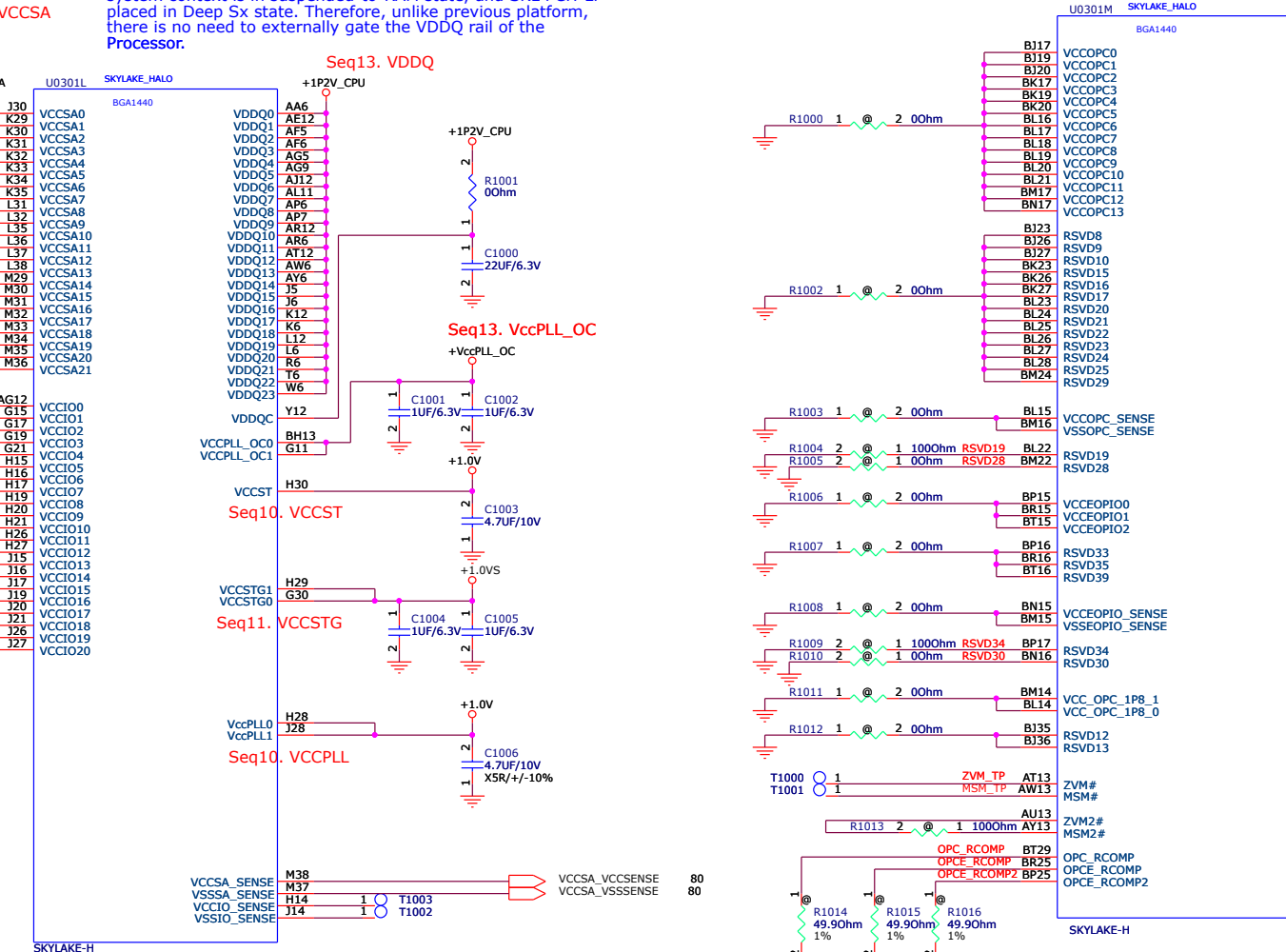
Seq13. VccPLL\_OC

Seq10. VCCST

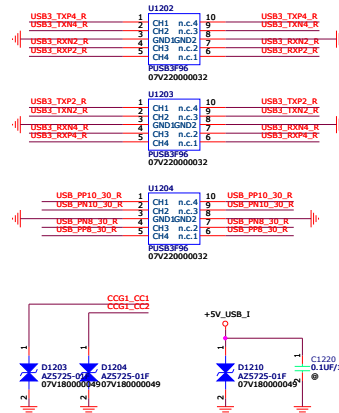
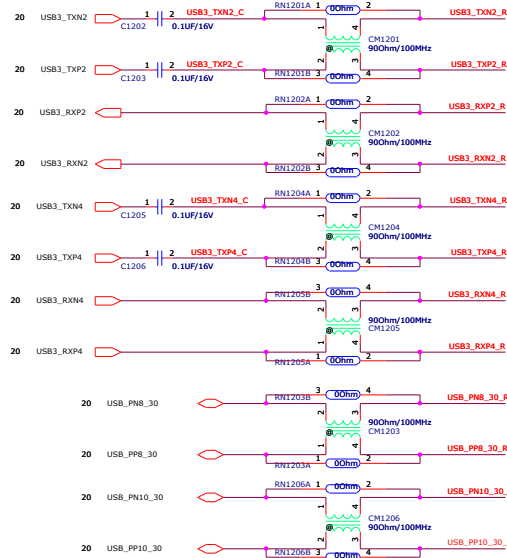
Seq11. VCCSTG

Seq10. VCCPLL

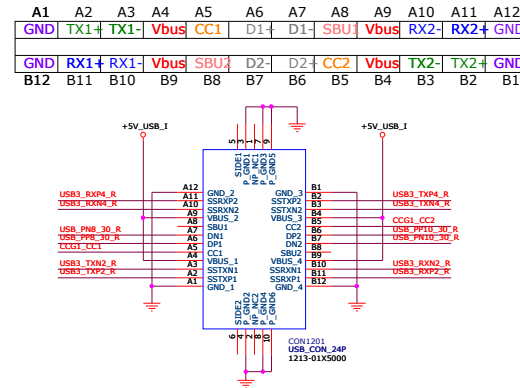
+VCCSA 80  
 +VCCIO 3,6,7,94  
 +1P2V 5,7,16,24,57,83



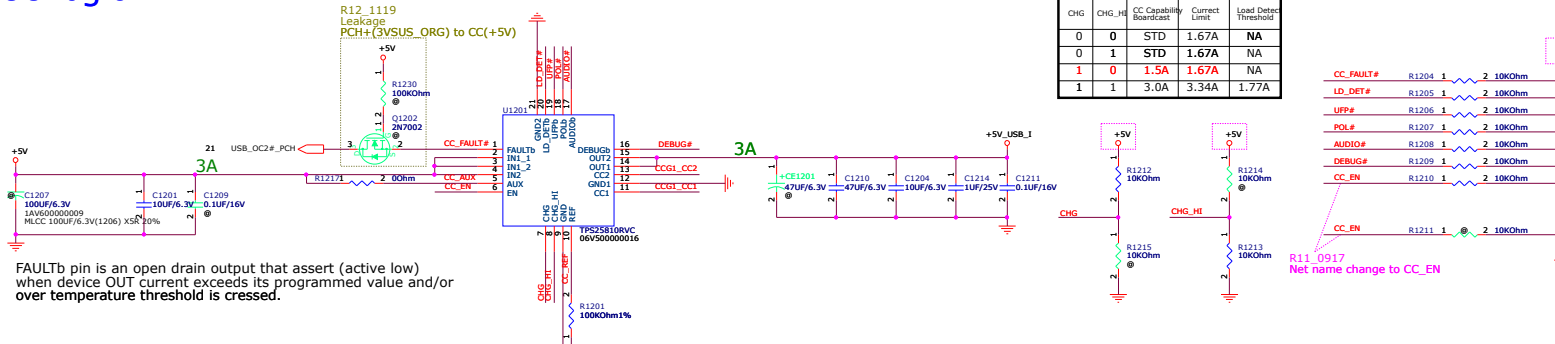
## Type-C

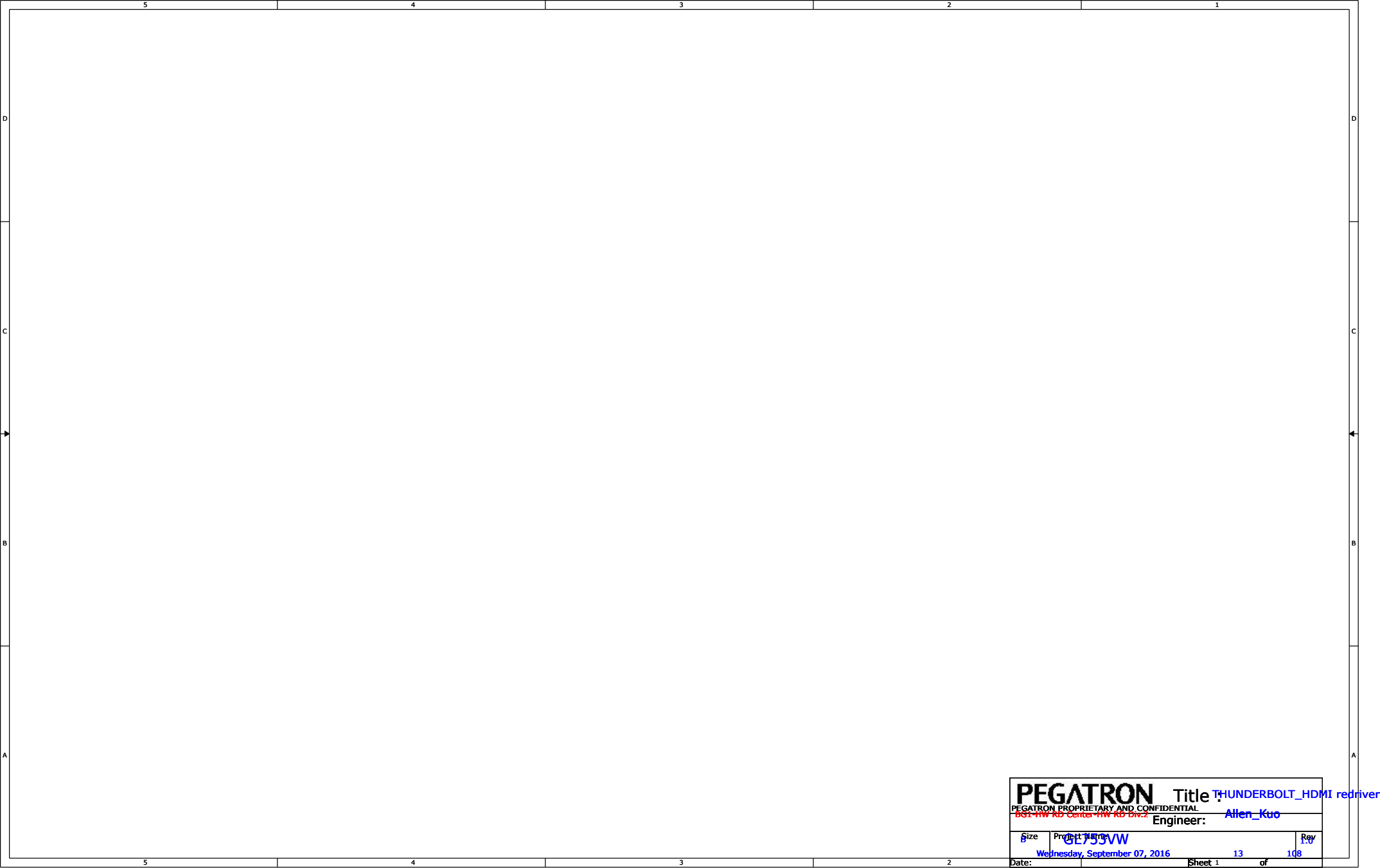


## Type-C Conn.



## CC logic





PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

061-HW RD Center HW RD Div.2

Size

Project Name

Date:

Rev

Project Name

Wednesday, September 07, 2016

Title

THUNDERBOLT\_HDMI redriver

Engineer:

Allen\_Kuo

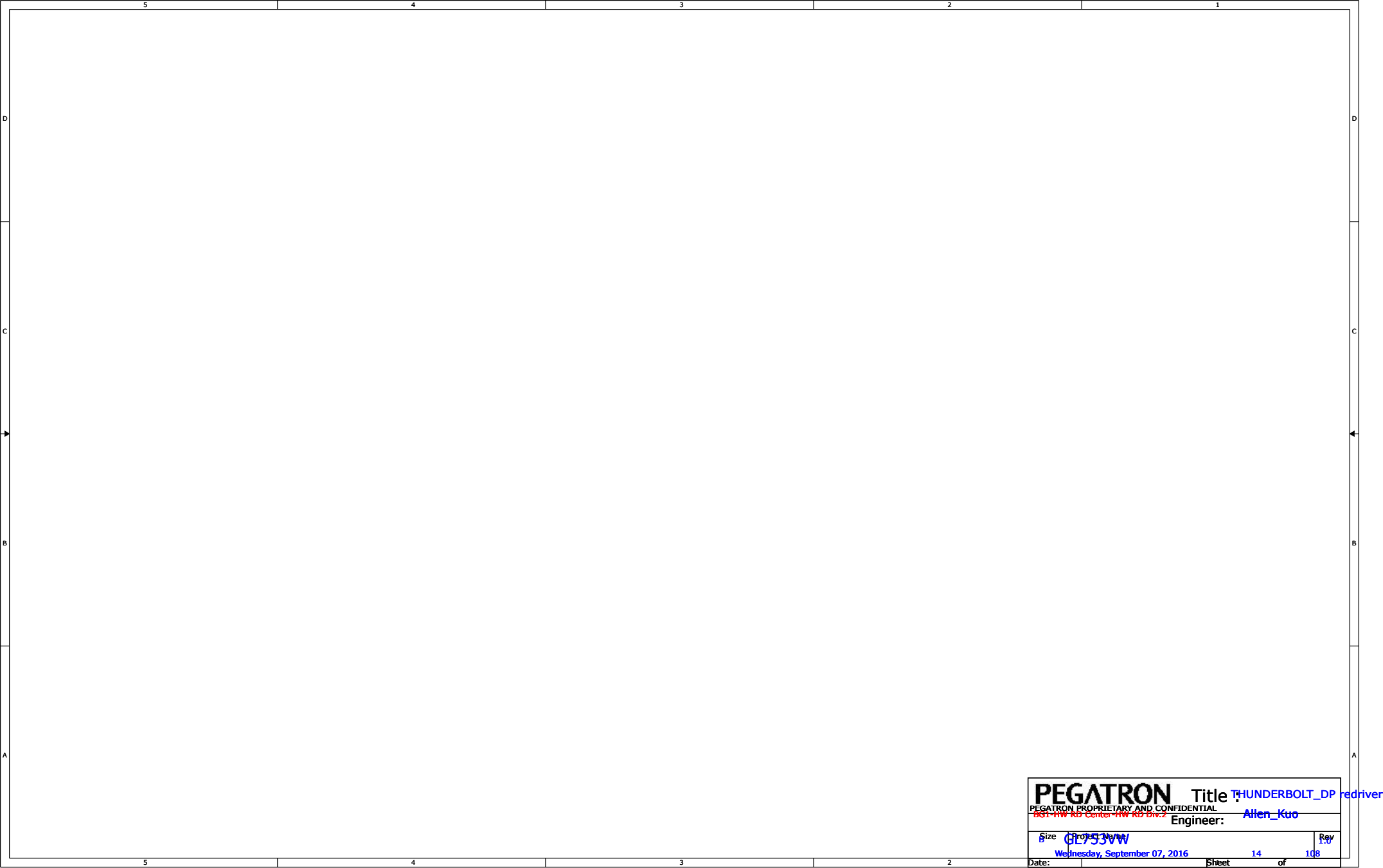
Sheet 1

of

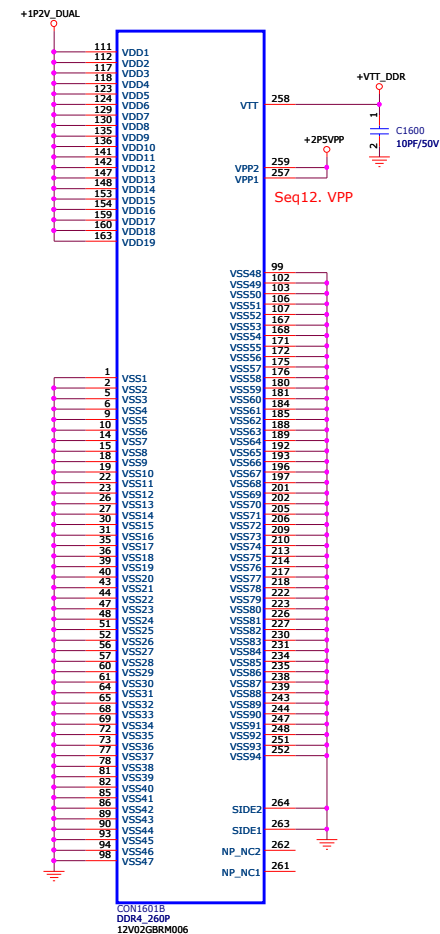
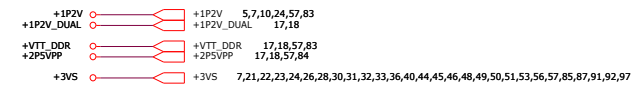
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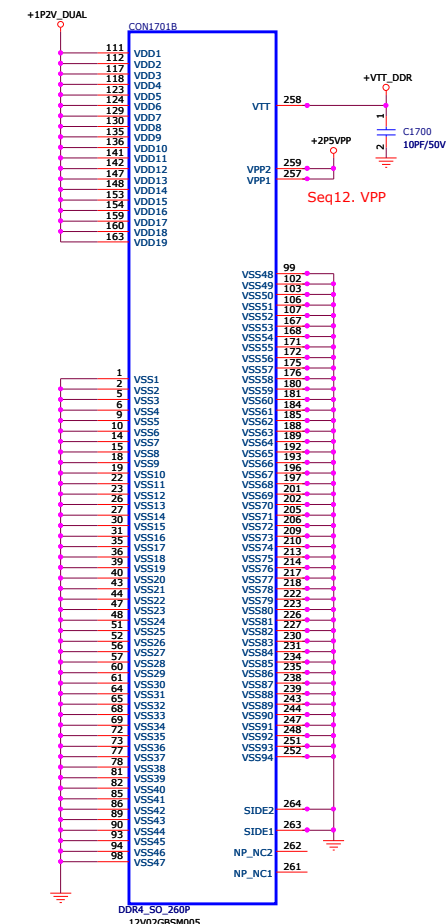
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1.0

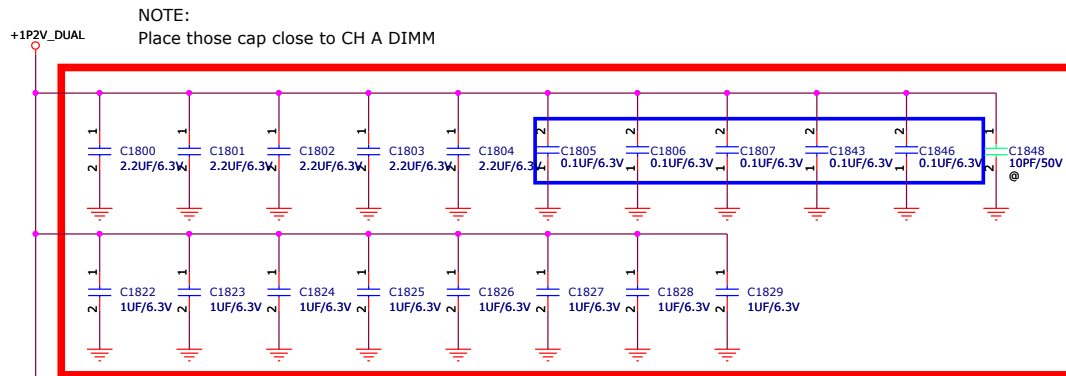


<b>PEGATRON</b>		Title: <b>THUNDERBOLT_DP</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL		Engineer: <b>Allen_Kuo</b>	
Size: <b>GL933WV</b>	Project Name: <b>GL933WV</b>	Rev: <b>1.0</b>	
Date: <b>Wednesday, September 07, 2016</b>	Sheet: <b>14</b>	of: <b>108</b>	



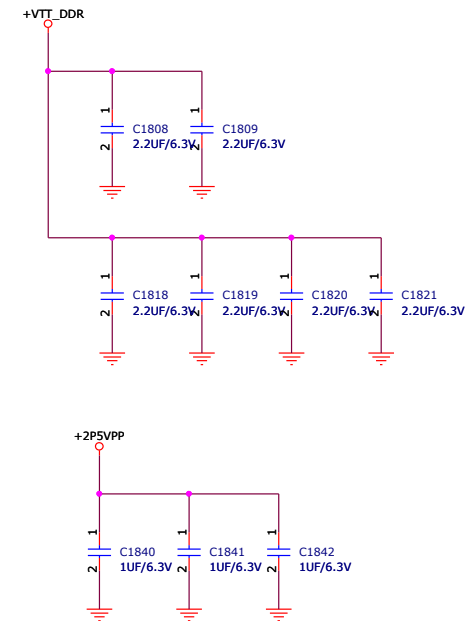
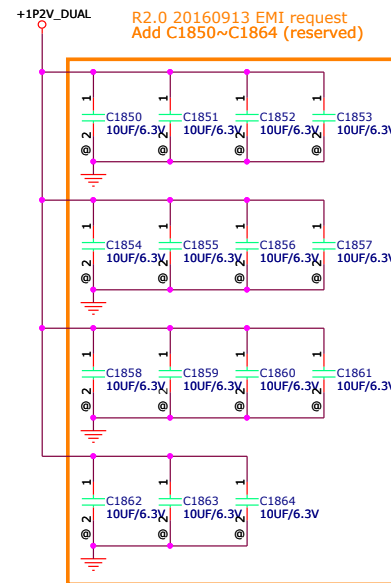
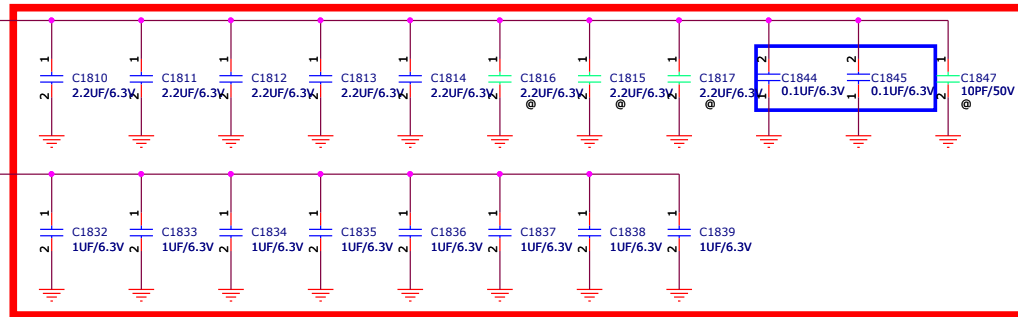






NOTE:  
Place those cap close to CH B DIMM

R1.2 20160728 EMI request  
Mount C1805, C1806, C1807, C1843, C1844, C1845, C1846  
(0.1 uF)



### DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x $\mu$ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 $\mu$ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 $\mu$ F (0402)	
		1 placeholder	1x 330 $\mu$ F (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10 $\mu$ F (0603)	
		Placeholder	1x 10 $\mu$ F (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1 $\mu$ F (0402)	
	VPP	DRAM Side	2x 10 $\mu$ F (0603)	
		DRAM Side	2x 1 $\mu$ F (0402)	
	VDDSPD	Place close to DIMM	1x 0.1 $\mu$ F (0402)	
		Place close to DIMM	1x 22 $\mu$ F (0402)	

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HDD  
SATA port

ODD  
SATA port

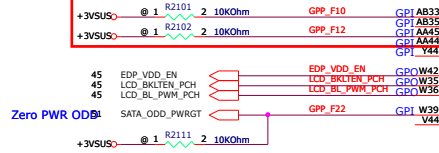
NOTE:

SATAxPCIE[0:7]	SATA/PCIE
SATAxPCIE0	SATA0A/PCIE9
SATAxPCIE1	SATA1B/PCIE10
SATAxPCIE2	SATA2/PCIE15
SATAxPCIE3	SATA3/PCIE16
SATAxPCIE4	SATA4/PCIE17
SATAxPCIE5	SATA5/PCIE18
SATAxPCIE6	SATA5/PCIE19
SATAxPCIE7	SATA7/PCIE20

20160310  
20160315

56 AIR\_LED  
53 WLAN\_ON  
53 BT\_ON/OFF#  
56 BT\_LED

546884\_SKL\_PDG\_H\_rev2\_0 p662  
All unused GPIOs (which default to GPIO functionality) do not need termination.



### PCIE/SATA

B36 PCIE13\_TXP/SATA0B\_TXP  
C38 PCIE13\_TXN/SATA0B\_TXN  
E35 PCIE13\_RXP/SATA0B\_RXP  
G39 PCIE13\_RXN/SATA0B\_RXN

A30 PCIE15\_TXP/SATA2\_TXP  
B39 PCIE15\_TXN/SATA2\_TXN  
F41 PCIE15\_RXP/SATA2\_RXP  
F41 PCIE15\_RXN/SATA2\_RXN

A40 PCIE16\_TXP/SATA3\_TXP  
A41 PCIE16\_TXN/SATA3\_TXN  
D43 PCIE16\_RXP/SATA3\_RXP  
D43 PCIE16\_RXN/SATA3\_RXN

F45 PCIE17\_TXP/SATA4\_TXP  
H40 PCIE17\_TXN/SATA4\_TXN  
H42 PCIE17\_RXP/SATA4\_RXP  
H42 PCIE17\_RXN/SATA4\_RXN

G44 PCIE18\_TXP/SATA5\_TXP  
G37 PCIE18\_TXN/SATA5\_TXN  
K37 PCIE18\_RXP/SATA5\_RXP  
K37 PCIE18\_RXN/SATA5\_RXN

H44 PCIE19\_TXP/SATA6\_TXP  
H43 PCIE19\_TXN/SATA6\_TXN  
L39 PCIE19\_RXP/SATA6\_RXP  
L39 PCIE19\_RXN/SATA6\_RXN

J45 PCIE20\_TXP/SATA7\_TXP  
K44 PCIE20\_TXN/SATA7\_TXN  
N38 PCIE20\_RXP/SATA7\_RXP  
N39 PCIE20\_RXN/SATA7\_RXN

GPI\_AB41 GPP\_F5/DEVSLP3  
GPI\_AB42 GPP\_F6/DEVSLP4  
GPI\_AB43 GPP\_F7/DEVSLP5  
GPI\_AB36 GPP\_F8/DEVSLP6  
GPI\_AB39 GPP\_F9/DEVSLP7

GPI\_AB33 GPP\_F10/SCLOCK  
GPI\_AB35 GPP\_F11/SLD  
GPI\_AA45 GPP\_F12/SDATAOUT1  
GPI\_AA46 GPP\_F13/SDATAOUT0  
GPI\_AA47 GPP\_F14

GPI\_W43 GPP\_F19/eDP\_VDDEN  
GPI\_W35 GPP\_F20/eDP\_BKLTEN  
GPI\_W36 GPP\_F21/eDP\_BKLTCTL  
GPI\_W39 GPP\_F22  
GPI\_V44 GPP\_F23

SKYLARK\_PCH

GPP\_E0/SATAxPCIE0/SATAGP0  
GPP\_E1/SATAxPCIE1/SATAGP1  
GPP\_E2/SATAxPCIE2/SATAGP2

AG36 PCIE\_SSD\_PEDET  
AG35 SATAGP1  
AG39 SATA\_ODD\_PRSNT#\_R

GPP\_E3/CPU\_GPO  
GPP\_E4/DEVSLP0  
GPP\_E5/DEVSLP1  
GPP\_E6/DEVSLP2  
GPP\_E7/CPU\_GPI  
GPP\_E8/SATALED#

GPP\_E9/USB2\_OC1#  
GPP\_E10/USB2\_OC1#  
GPP\_E11/USB2\_OC1#  
GPP\_E12/USB2\_OC1#

GPP\_F15/USB2\_OCB#  
GPP\_F16/USB2\_OCB#  
GPP\_F17/USB2\_OCB#  
GPP\_F18/USB2\_OCB#

GPP\_I0/DDPB\_HPD#  
GPP\_I1/DDPC\_HPD#  
GPP\_I2/DDPD\_HPD#  
GPP\_I3/DDPE\_HPD#  
GPP\_I4/EDP\_HPD#

GPP\_I5/DDPB\_CTRLCLK#  
GPP\_I6/DDPB\_CTRLCLK#  
GPP\_I7/DDPC\_CTRLCLK#  
GPP\_I8/DDPC\_CTRLCLK#  
GPP\_I9/DDPD\_CTRLCLK#  
GPP\_I10/DDPD\_CTRLCLK#

GPP\_F0/SATAxPCIE3/SATAGP3  
GPP\_F1/SATAxPCIE4/SATAGP4  
GPP\_F2/SATAxPCIE5/SATAGP5  
GPP\_F3/SATAxPCIE6/SATAGP6  
GPP\_F4/SATAxPCIE7/SATAGP7

GPP\_F19/eDP\_VDDEN  
GPP\_F20/eDP\_BKLTEN  
GPP\_F21/eDP\_BKLTCTL  
GPP\_F22  
GPP\_F23

+3VS

R2129 10KOhm

R2138 2 1 00hm

R2115 2 1 00hm

R2136 2 1 00hm

R2107 2 1 00hm

RN2101D 10KOhm

RN2101B 10KOhm

RN2101C 10KOhm

RN2101A 10KOhm

RN2101E 10KOhm

RN2101F 10KOhm

RN2101G 10KOhm

RN2101H 10KOhm

RN2101I 10KOhm

RN2101J 10KOhm

RN2101K 10KOhm

RN2101L 10KOhm

RN2101M 10KOhm

RN2101N 10KOhm

RN2101O 10KOhm

RN2101P 10KOhm

RN2101Q 10KOhm

RN2101R 10KOhm

RN2101S 10KOhm

RN2101T 10KOhm

RN2101U 10KOhm

RN2101V 10KOhm

RN2101W 10KOhm

RN2101X 10KOhm

PCIE\_SSD\_PEDET 51  
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SATA\_DEVSLP0 51  
SATA\_DEVSLP2 51  
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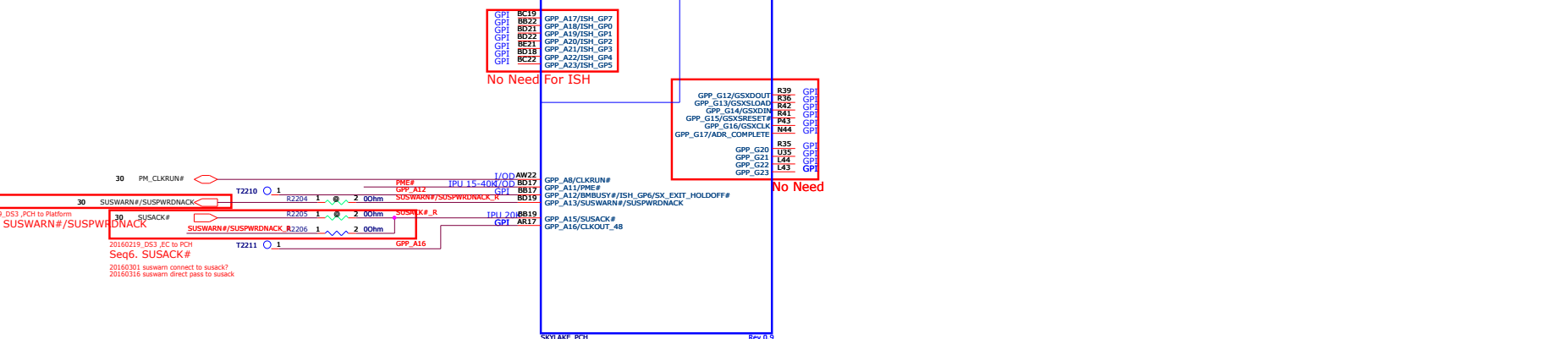
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USB\_OC2#\_PCH 12

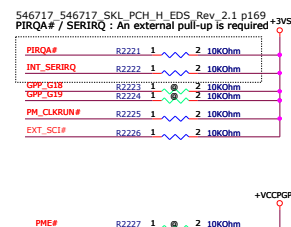
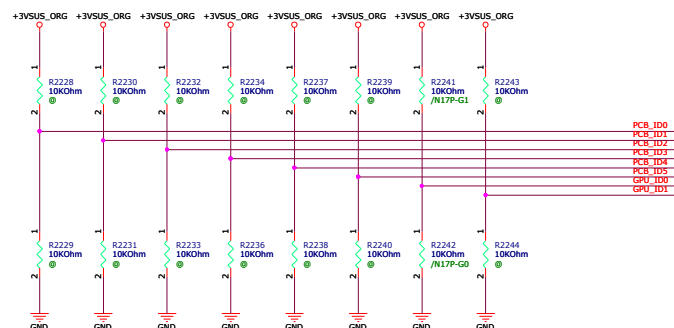
USB\_OC# 52  
USB\_OC1# 52  
USB\_OC2#\_PCH 12

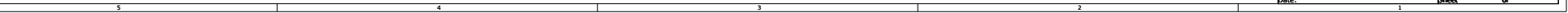
USB\_OC# 52  
USB\_OC1# 52  
USB\_OC2#\_PCH 12

USB\_OC# 52  
USB\_OC1# 52  
USB\_OC2#\_PCH 12



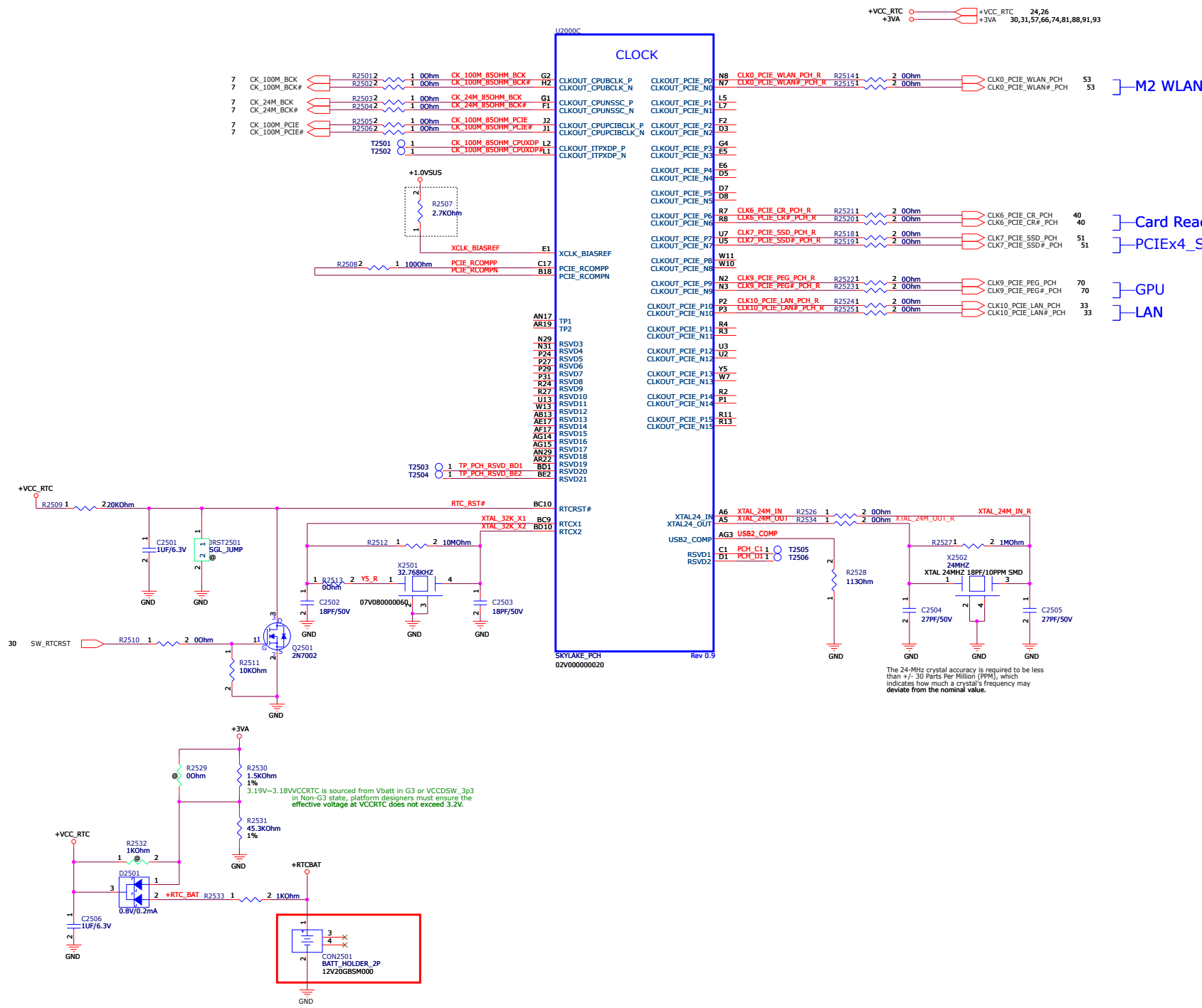
PCB_ID0	PCB_ID1	PCB_ID2	PCB_ID3	PCB_ID4	PCB_ID5	GPU_ID0	GPU_ID1
1: SATA SSD 0: PCIE SSD	1. AMIC 0. DMIC	1. Premium 0. Base	1: UMA 0: DSC	1: 2+2 0: 2+3e	1: SSD 0: nonSSD	1: N17P-G1 0: <b>N17P-G0</b>	1: TBD 0: TBD



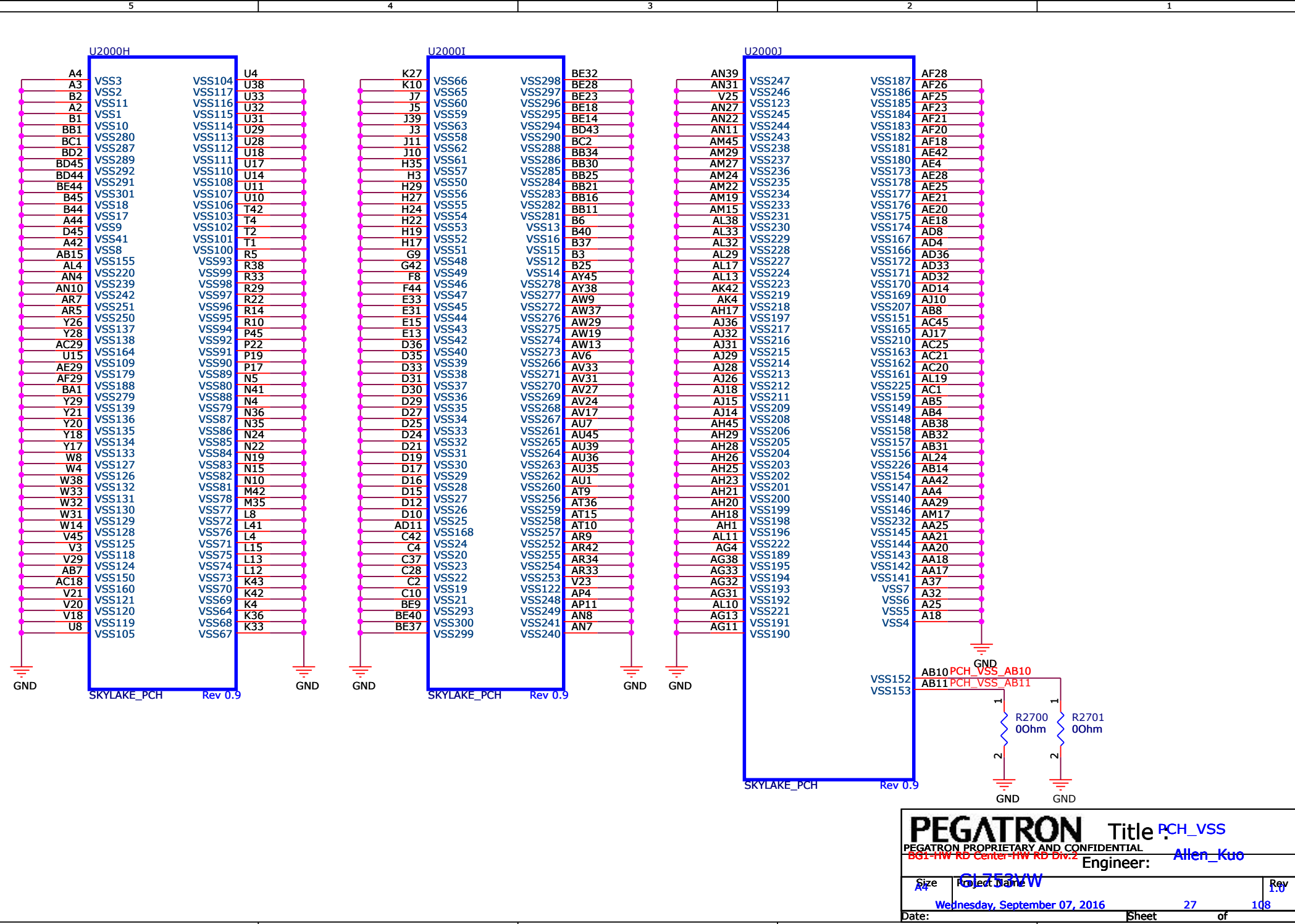




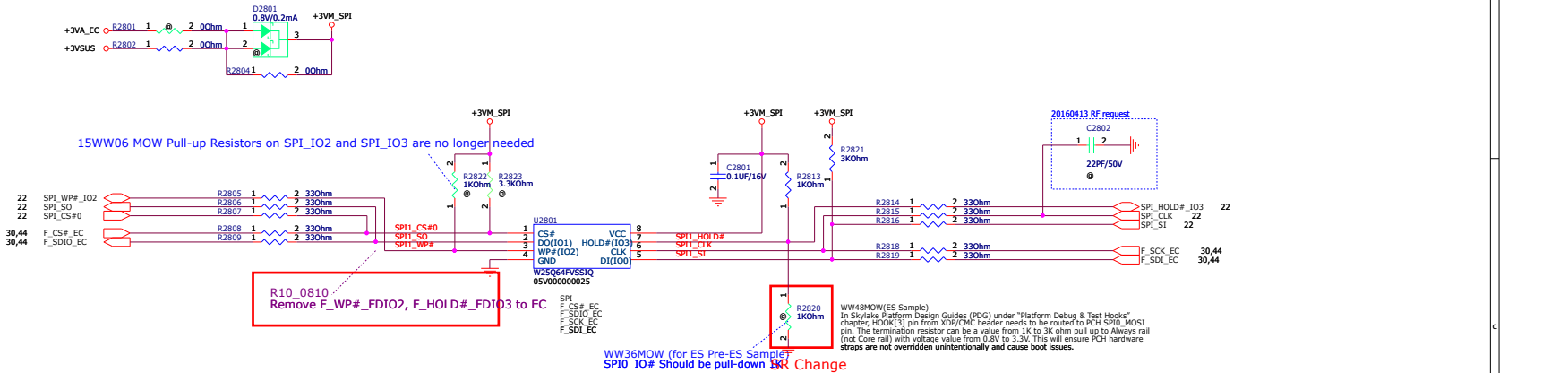




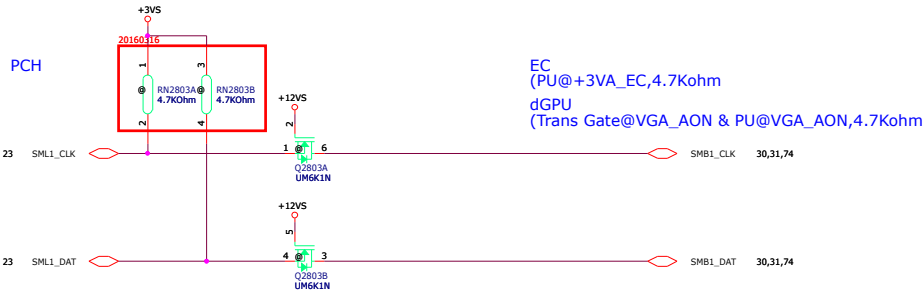
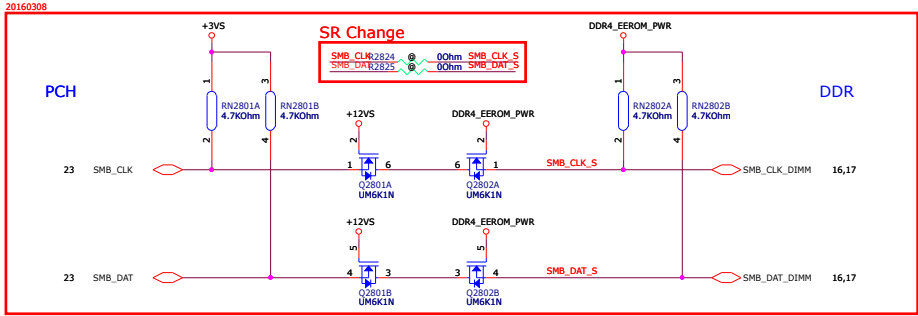
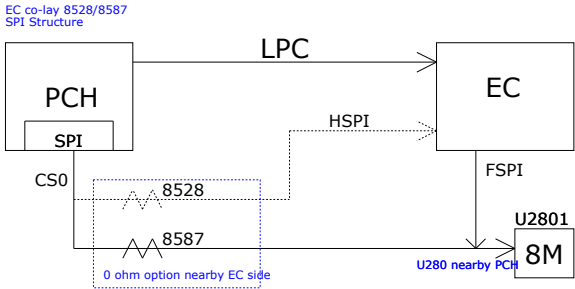




SPI ROM

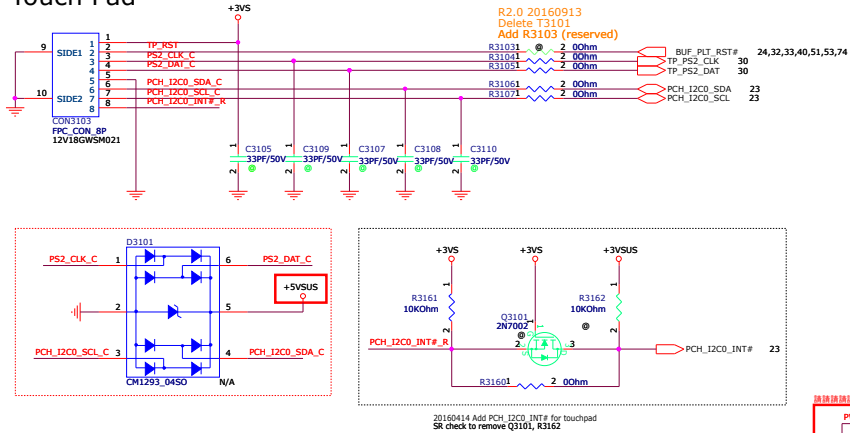


SMBus



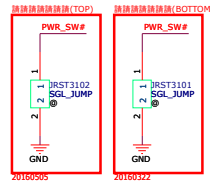


## Touch Pad

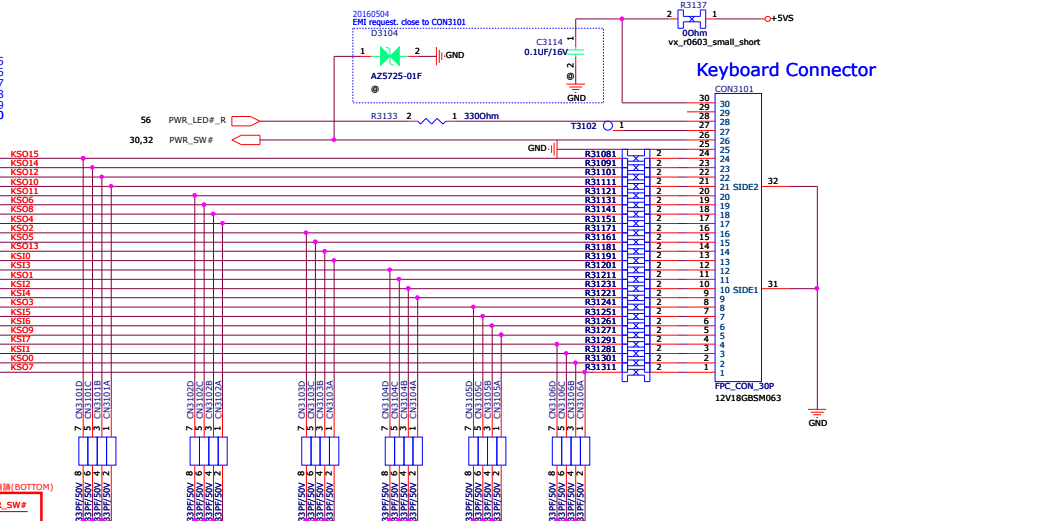


PWR SW 25  
PWR SW 26  
Caps LED 27  
PWR LED 28  
WIFI LED 29  
VCC=5V 30

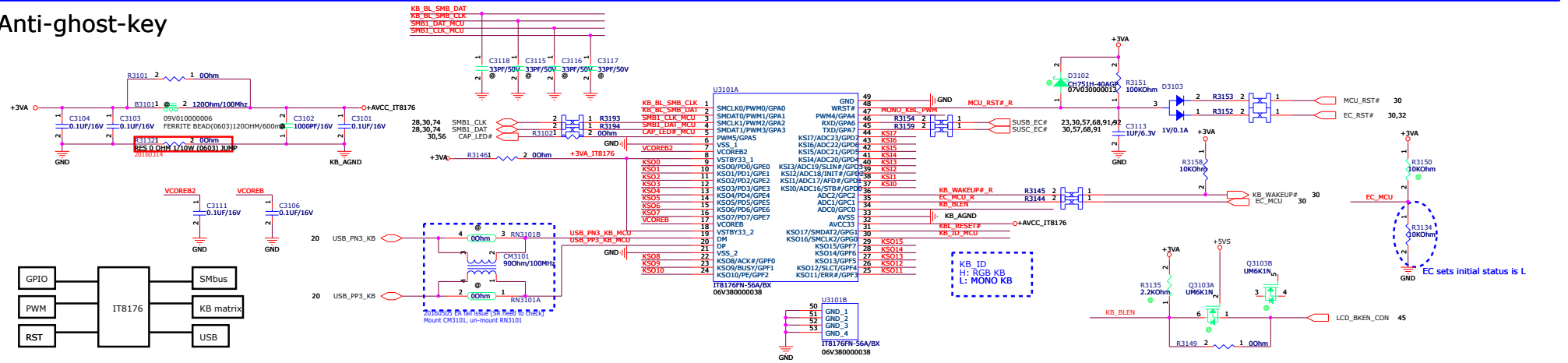
SUNREX



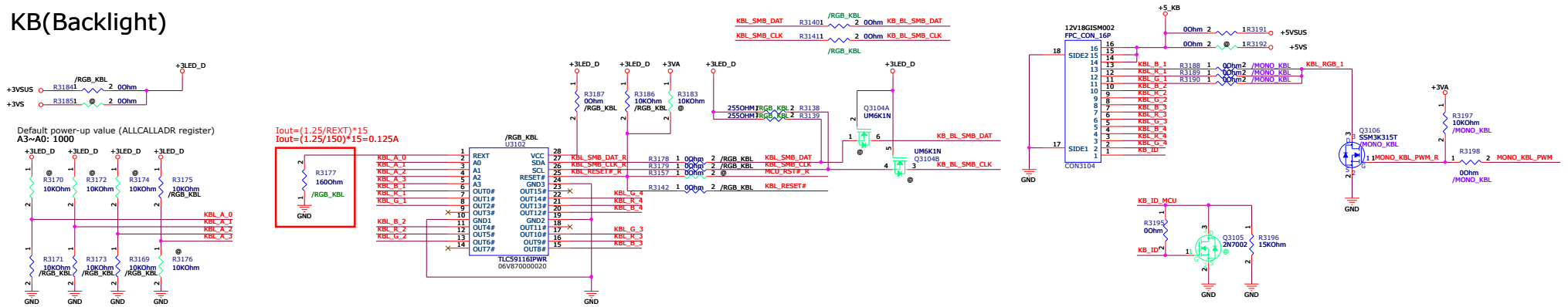
## Keyboard Connector



## Anti-ghost-key

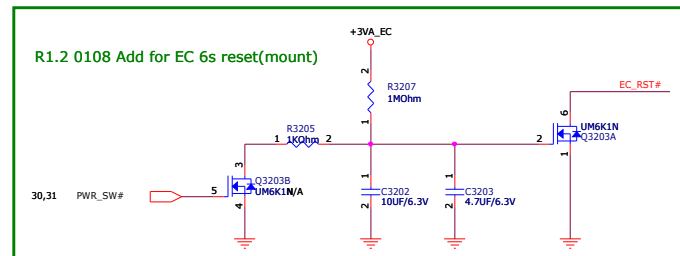
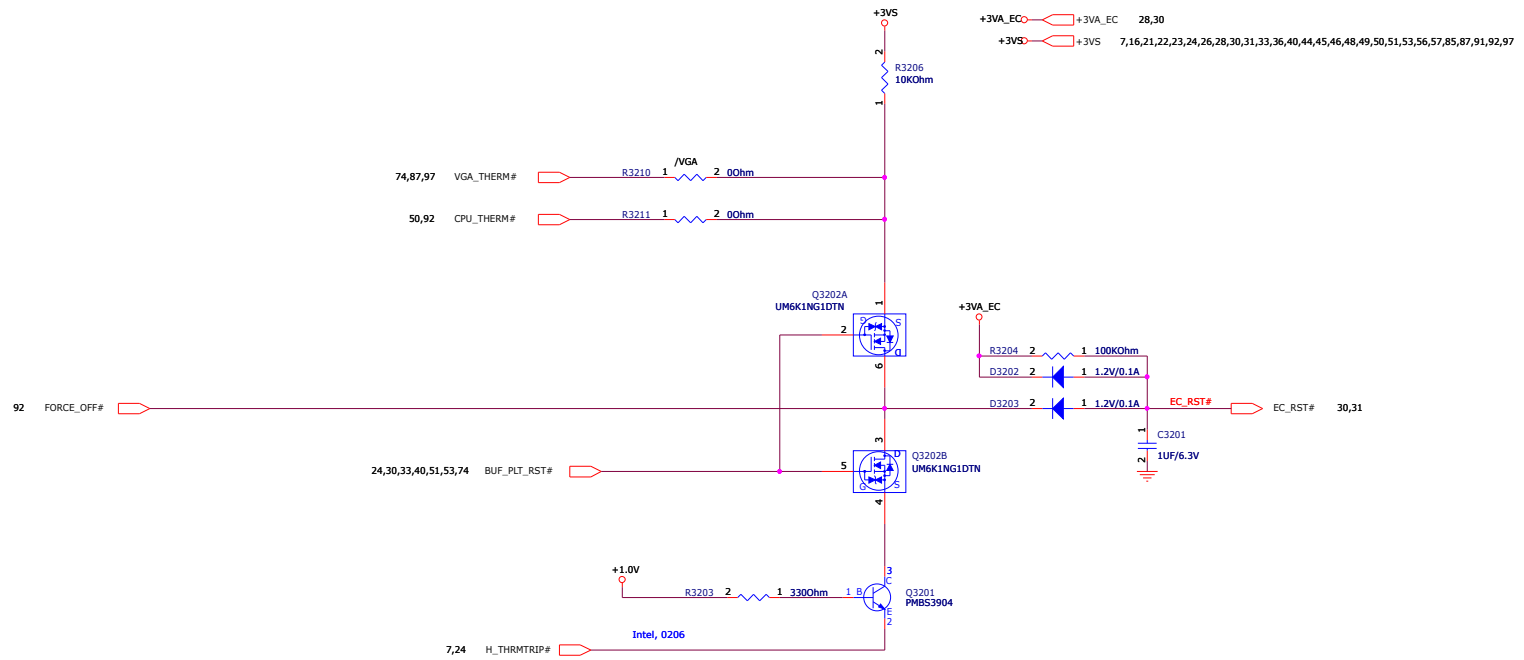


## KB(Backlight)

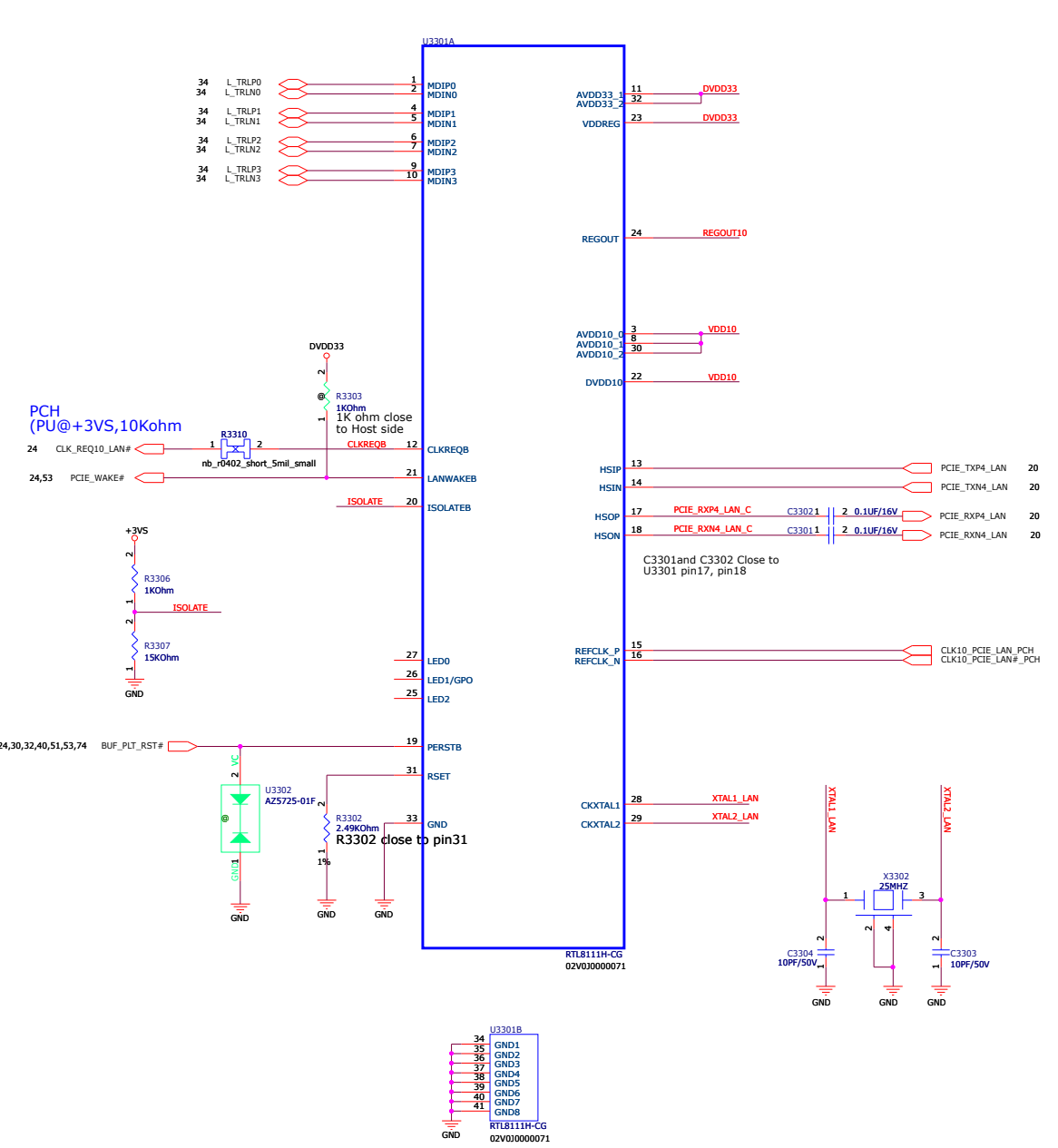




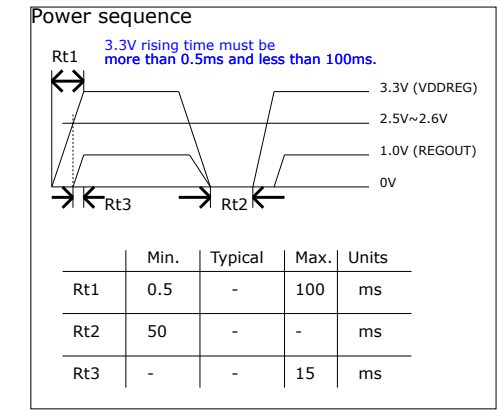
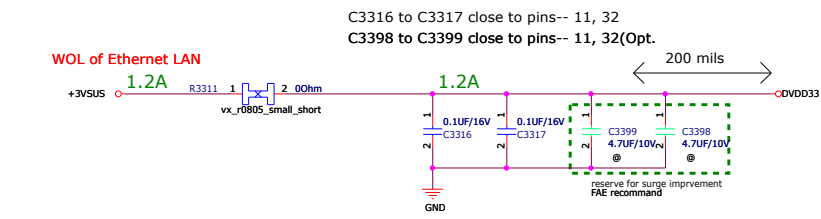
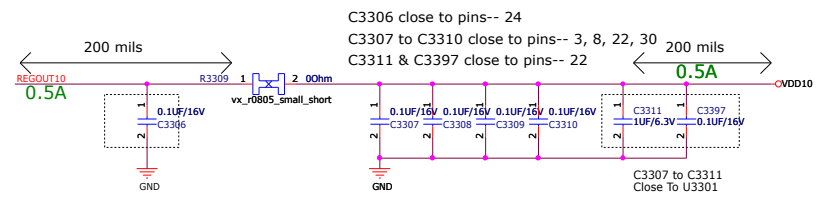
## Thermal Policy



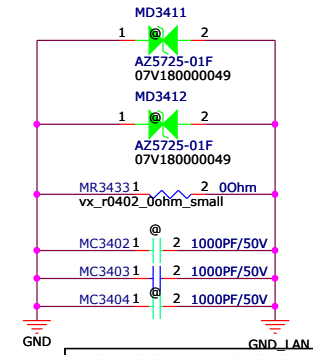
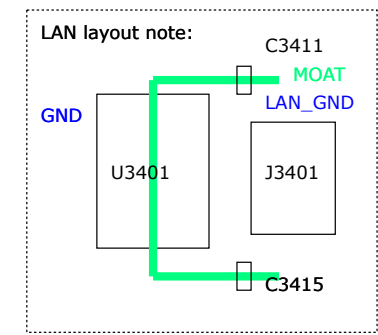
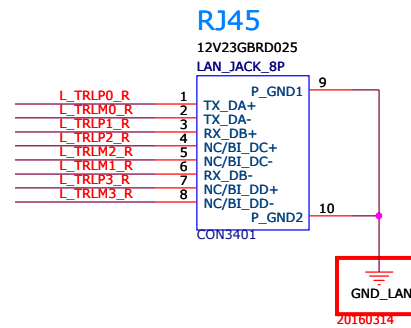
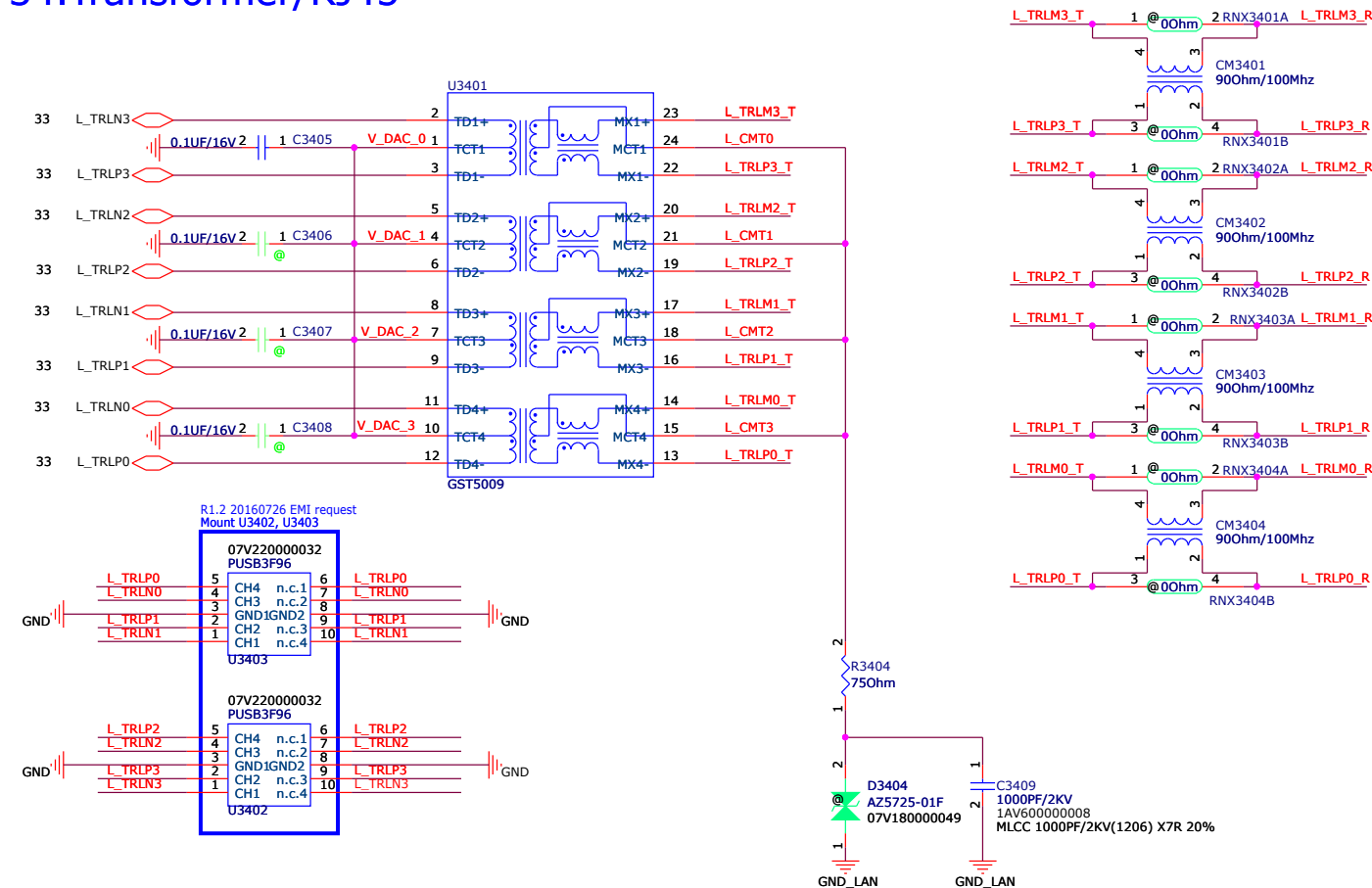
33.Realtek RTL8111H



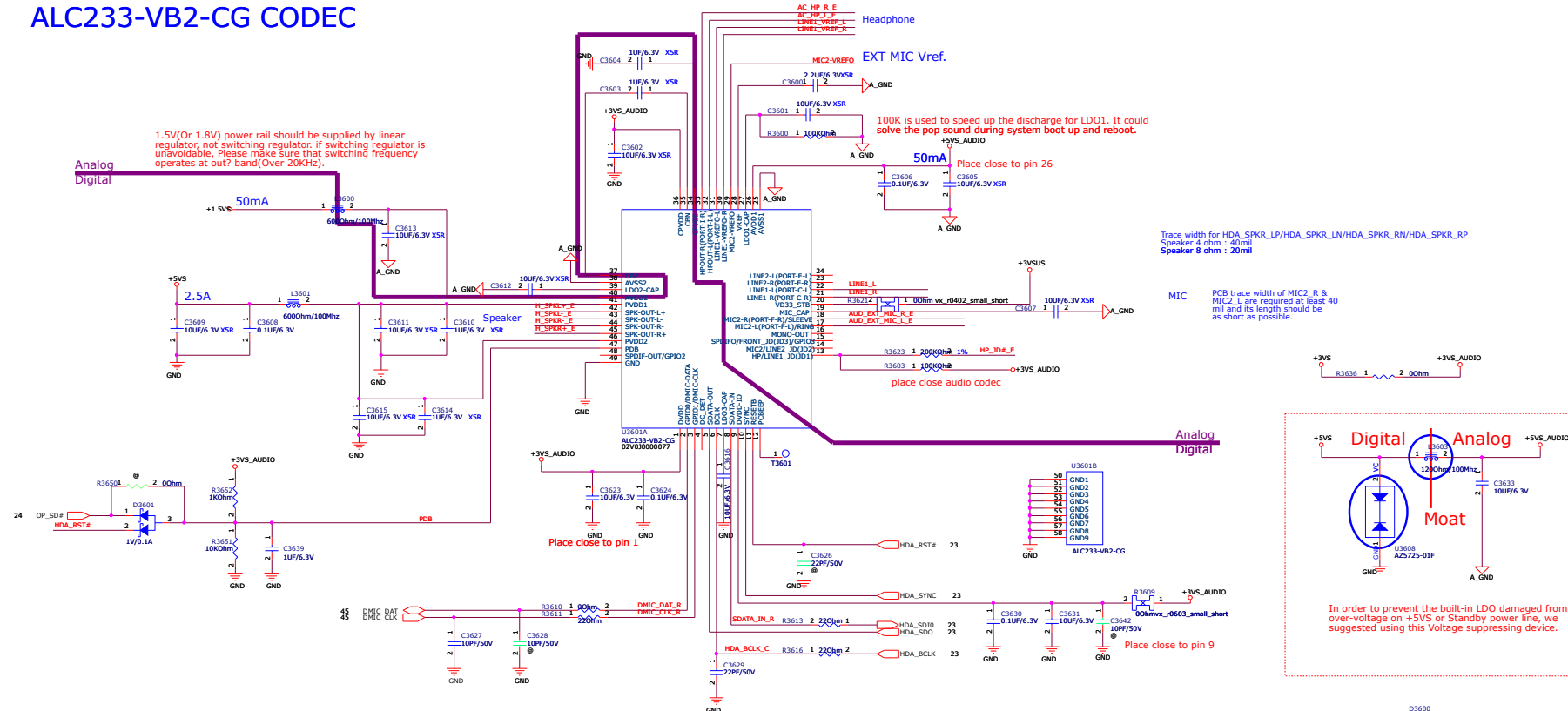
+3VS 7,16,21,22,23,24,26,28,30,31,32,36,40,44,45,46,48,49,50,51,53,56,57,85,87,91,92,97  
+3VSUS 7,21,23,24,26,28,30,31,36,44,68,74,81,92,97



### 34.Transformer/RJ45



## ALC233-VB2-CG CODEC

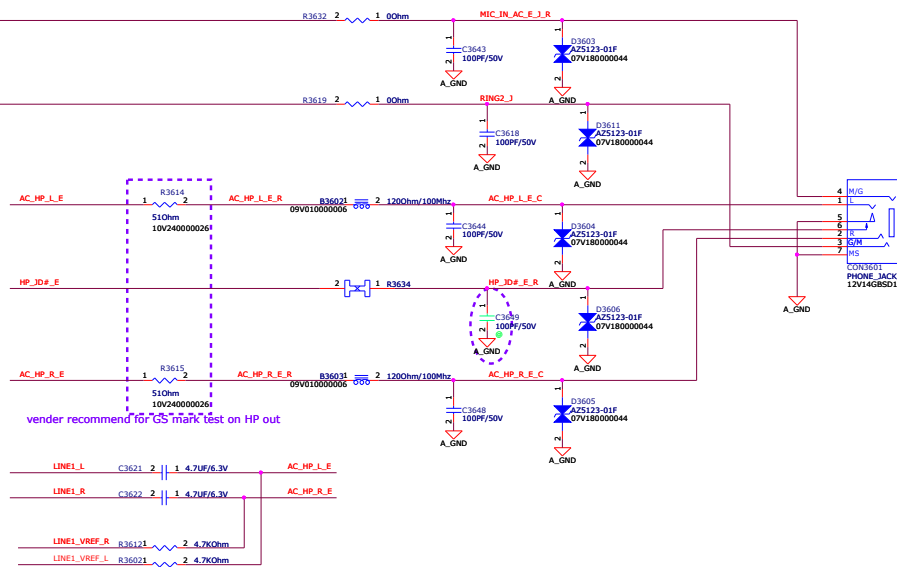


**MIC2-VREFO**

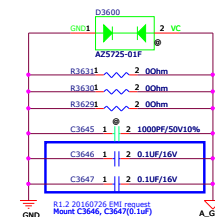
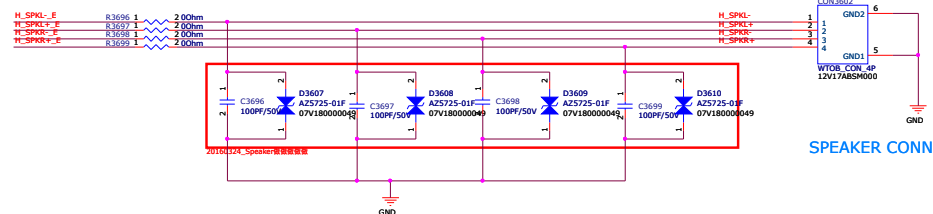
EXT MIC IN -

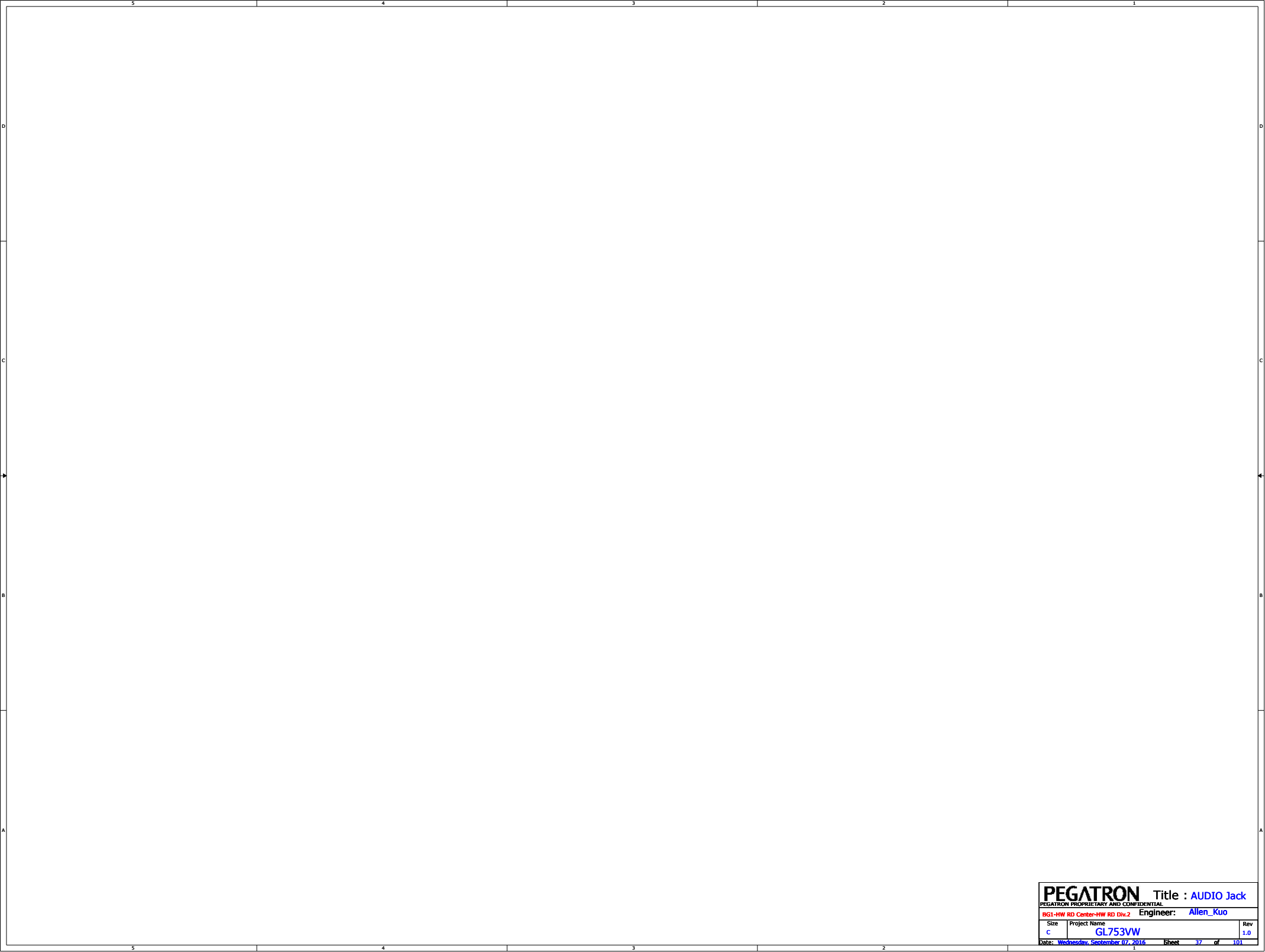
EXT FILE IN

## Combo Jack



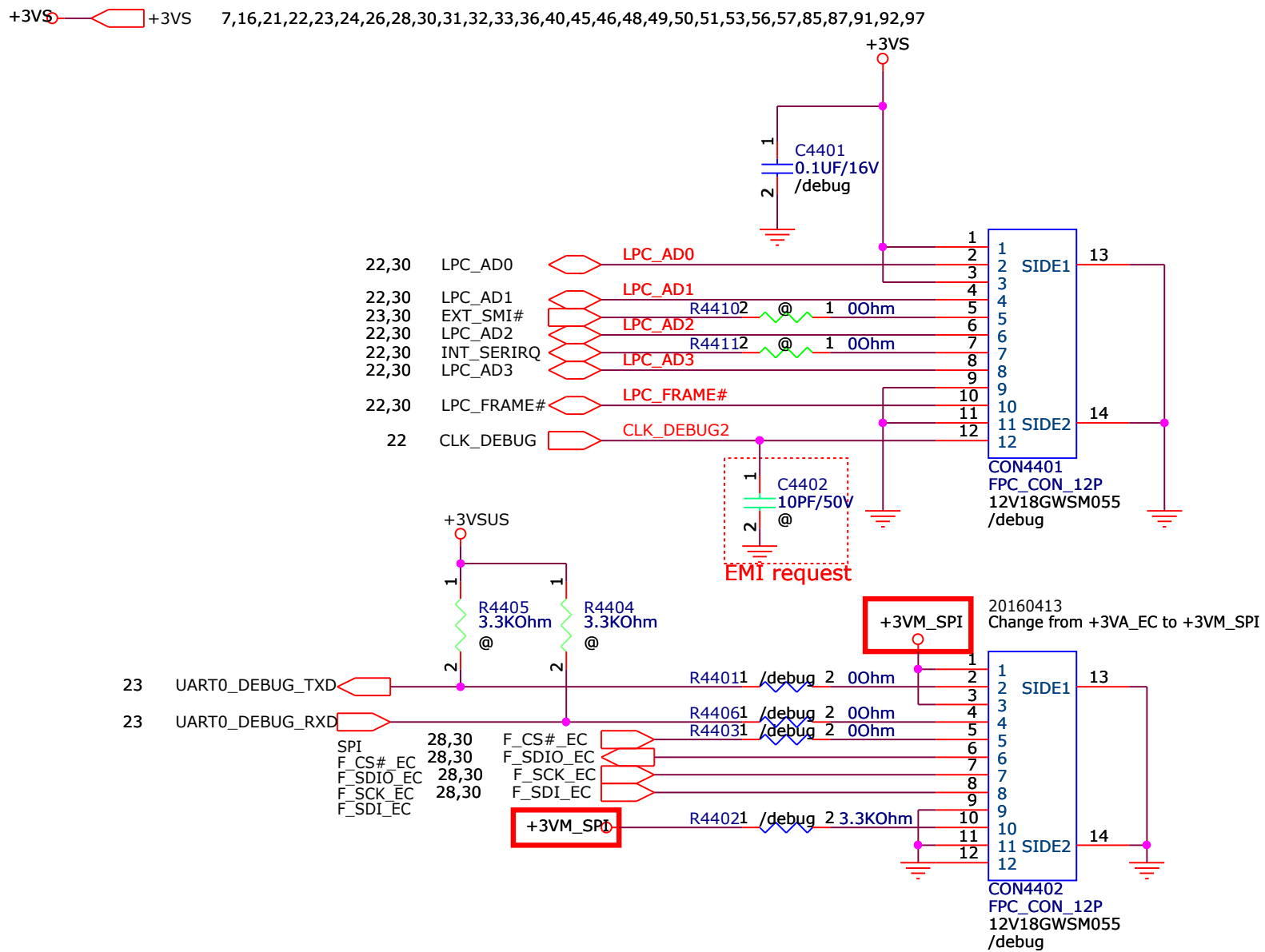
## SPKR Conn.







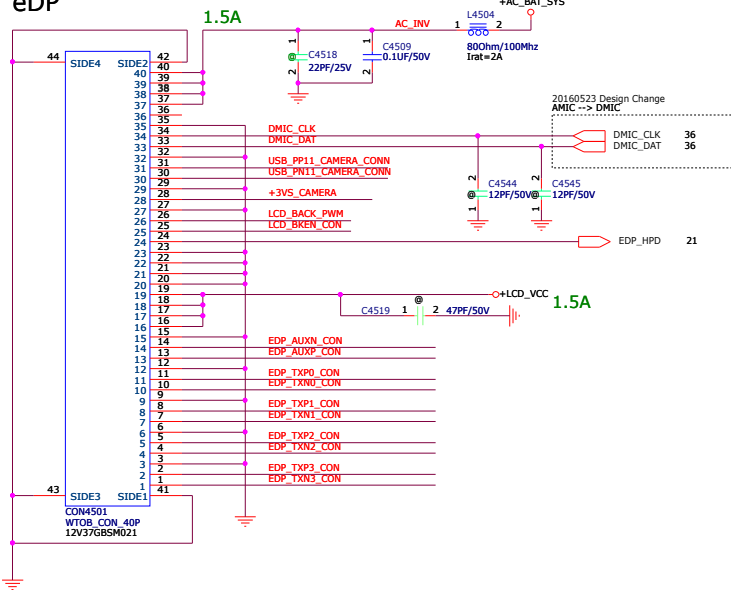




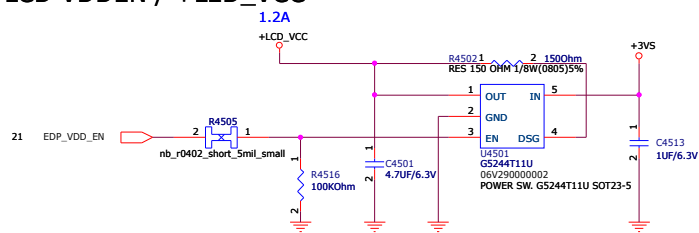
<Variant Name>

<b>PEGATRON</b>		Title: <b>DEBUG CON</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BGI-HW RD Center HW RD Div.2		Engineer: <b>Allen_Kuo</b>	
Size: <b>A</b>	Project Name: <b>GL753VW</b>	Rev: <b>1.0</b>	
Date: <b>Wednesday, September 07, 2016</b>		Sheet: <b>44</b>	of: <b>108</b>

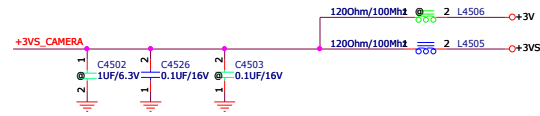
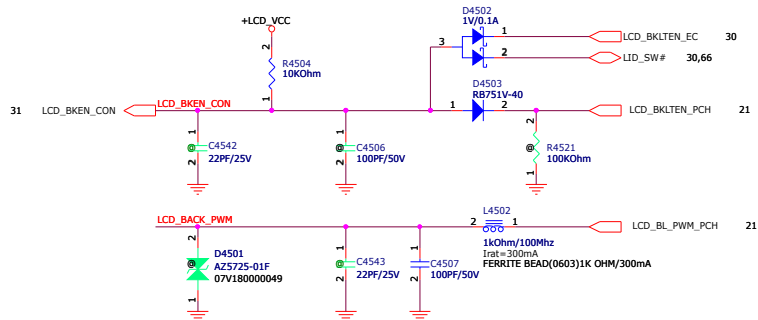
## eDP



## LCD VDDEN / +LED\_VCC



## Control Signal

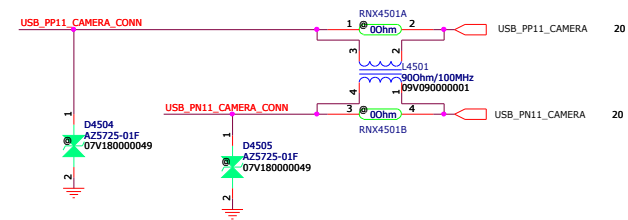


+3VS 7,16,21,22,23,24,26,28,30,31,32,33,36,40,44,46,48,49,50,51,53,56,57,85,87,91,92,97

+5VS 31,36,46,48,50,51,56,57,80,87,89,91,97

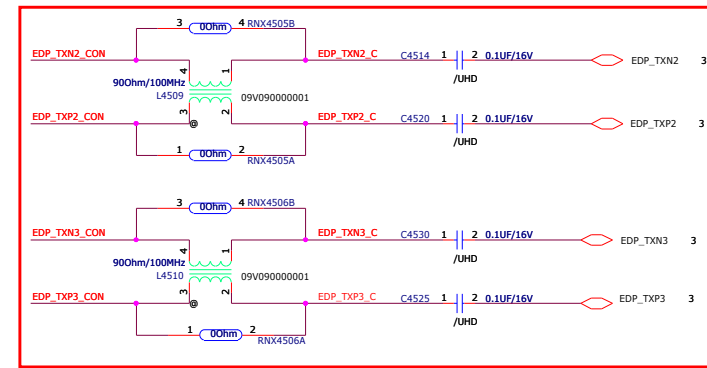
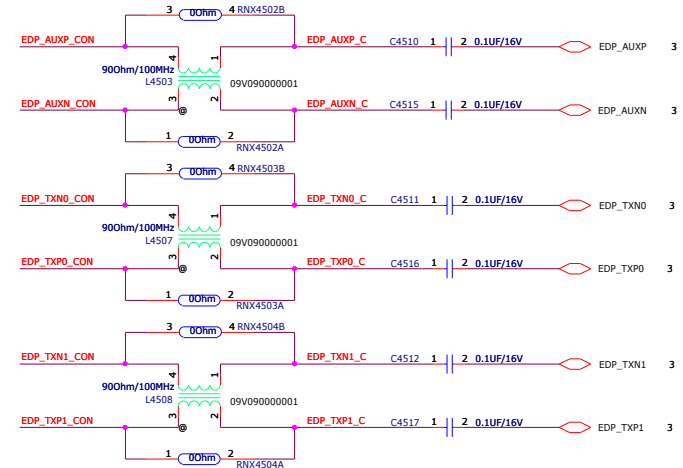
+AC\_BAT\_SYS 80,81,82,83,87,88,89,94,97

## Camera



546884\_SKL\_PDG\_H\_rev2\_0 p631

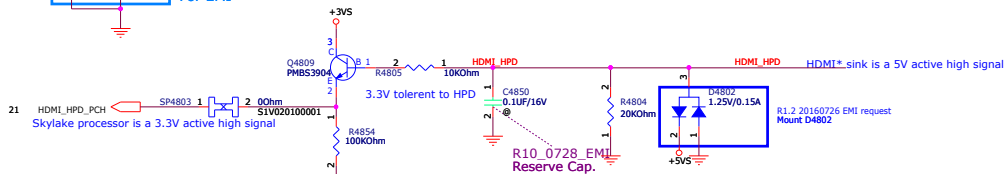
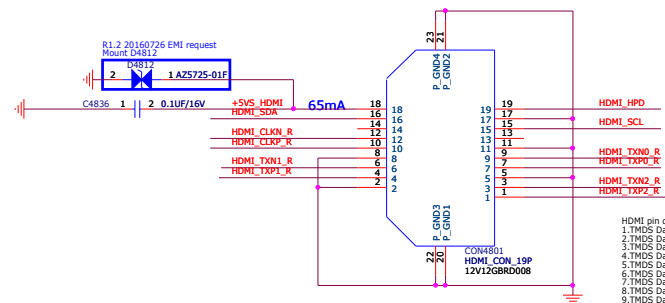
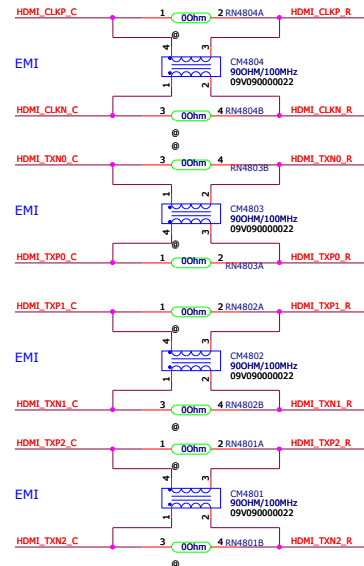
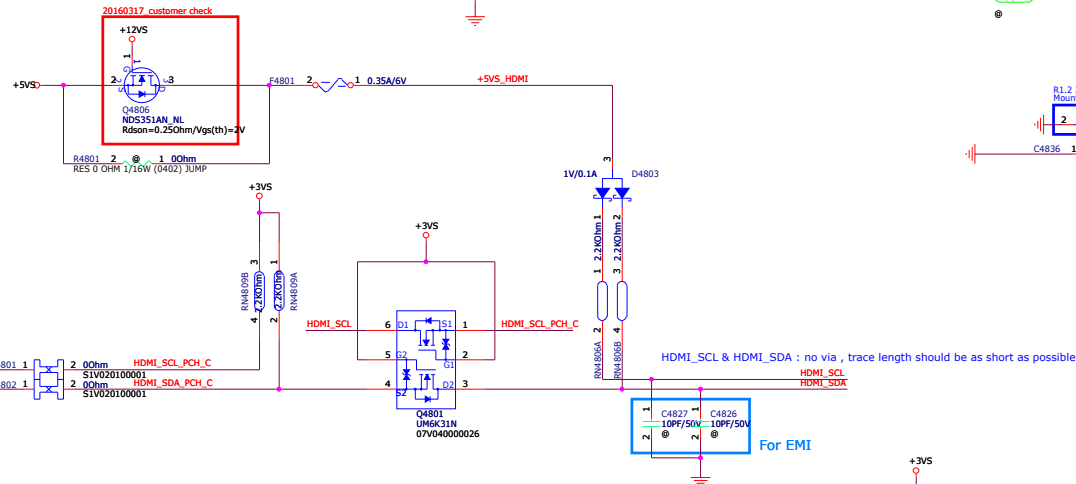
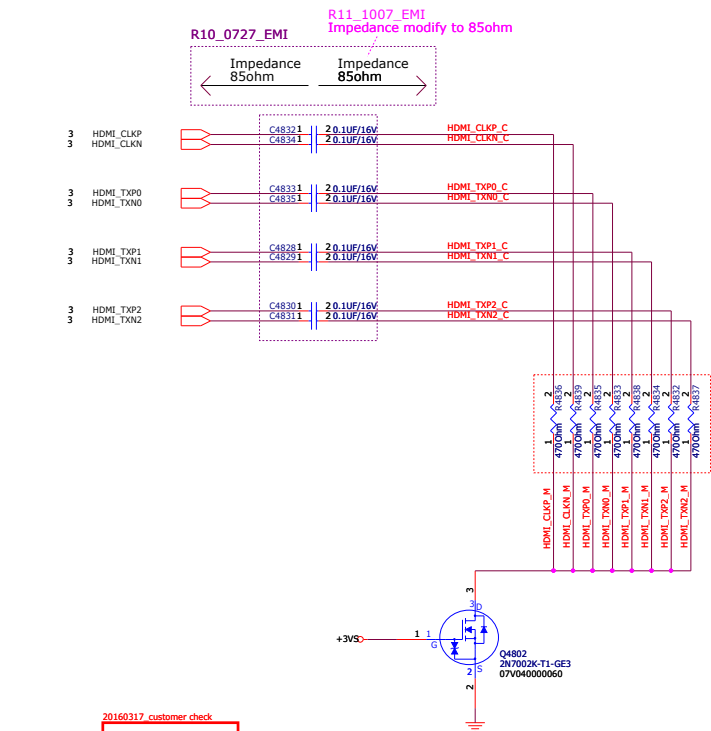
The path from the processor should be AC coupled using 75~200 nF capacitor






## UHD



## HDMI



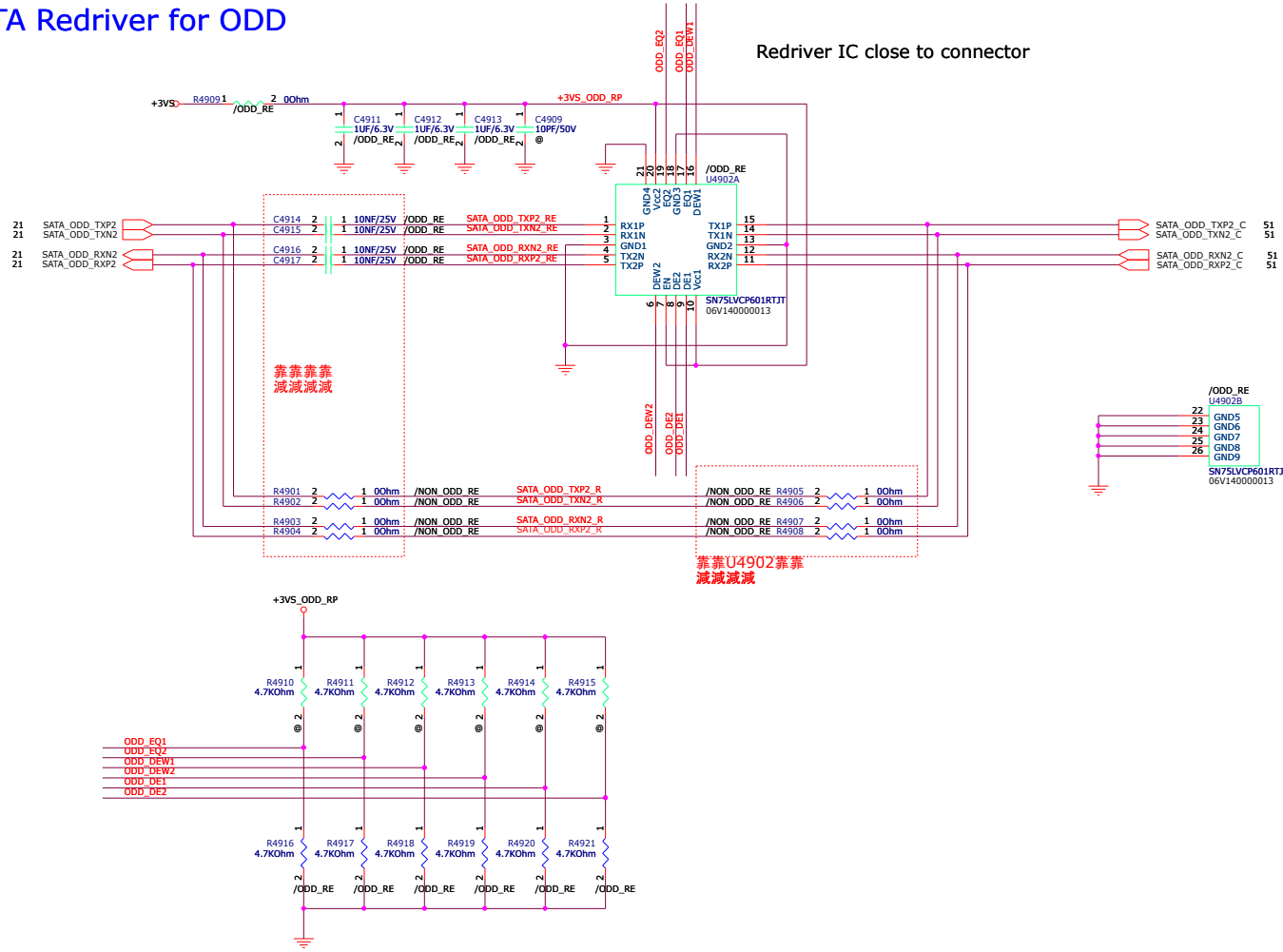
+3VS		+3VS	7,16,21,22,23,24,26,28,30,31,32,33,36,40,44,45,46,49,50,51,53,56,57,85,87,91,92,97
+5VS		+5VS	31,36,46,50,51,56,57,80,87,89,91,97
+12VS		+12VS	28,46,57,91

HDMI pin definition(Micro Type A)  
 1.TMDS Data2+  
 2.TMDS Data2- Shield  
 3.TMDS Data2-  
 4.TMDS Data1+  
 5.TMDS Data1- Shield  
 6.TMDS Data1-  
 7.TMDS Data0+  
 8.TMDS Data0- Shield  
 9.TMDS Data0-  
 10.TMDS Clock+  
 11.TMDS Clock Shield  
 12.TMDS Clock-  
 13.CEC  
 14.Reserve  
 15.SCL  
 16.SDA  
 17.DDC/CEC ground  
 18.+5V power  
 19.Hot plug detect

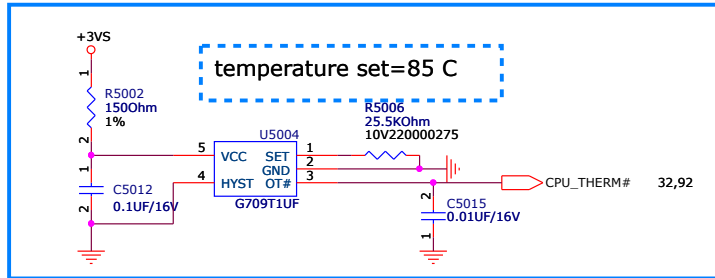
# SATA Redriver for ODD

+3VS 7,16,21,22,23,24,26,28,30,31,32,33,36,40,44,45,46,48,50,51,53,56,57,85,87,91,92,97

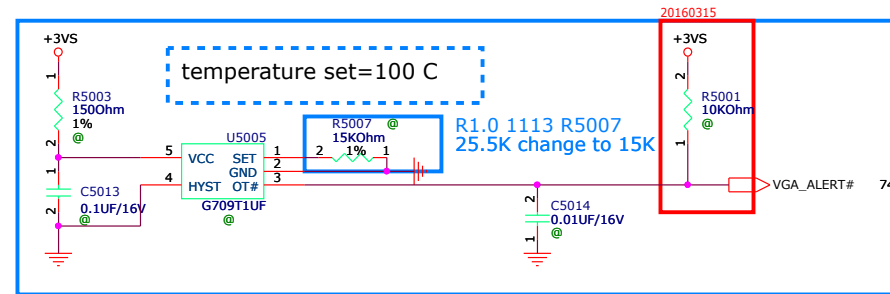
Redriver IC close to connector



## CPU Thermal Sensor



## GPU Thermal Sensor

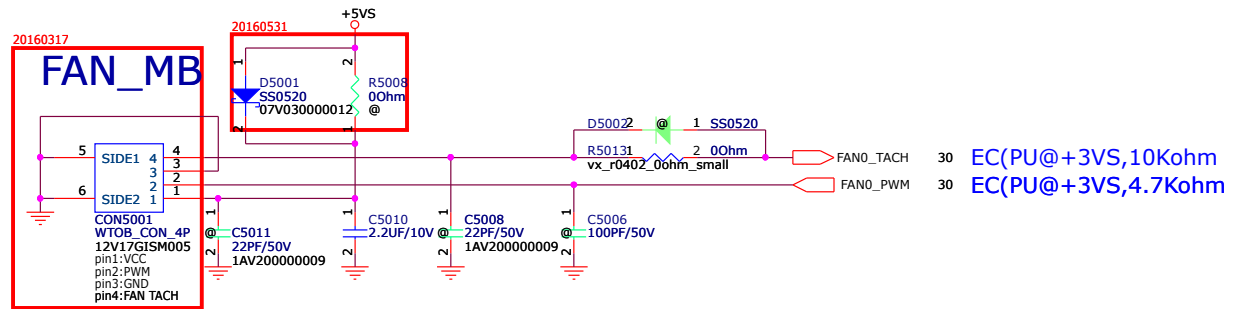


## FAN\_Module

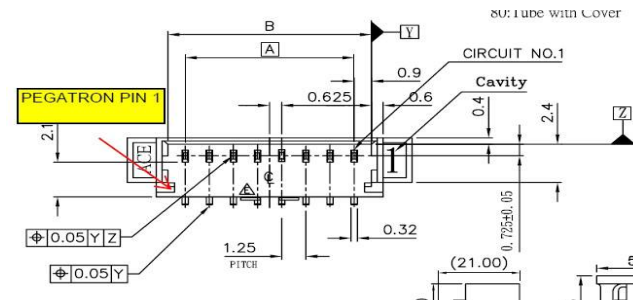
HOUSING P/N:Molex 51021-8604  
or EQUIVALENT

RED(紅)  
BLUE(藍)  
BLACK(黑)  
YELLOW(黃)  
UL3302 #28AWG OD=0.9mm  
+:RED(紅), -:BLACK(黑)  
3rd Wire:YELLOW(黃)  
4th PWM:BLUE(藍)

DETAIL A



teknisi-indonesia



<b>PEGATRON</b> Title: FAN/THERMAL	
PEGATRON PROPRIETARY AND CONFIDENTIAL	
Engineer: Allen_Kuo	
Size: 8	Project Name: GL753VW
Date: Monday, September 12, 2016	Sheet 50 of 108

NGFF socket M  
PCIEx4 SSD1

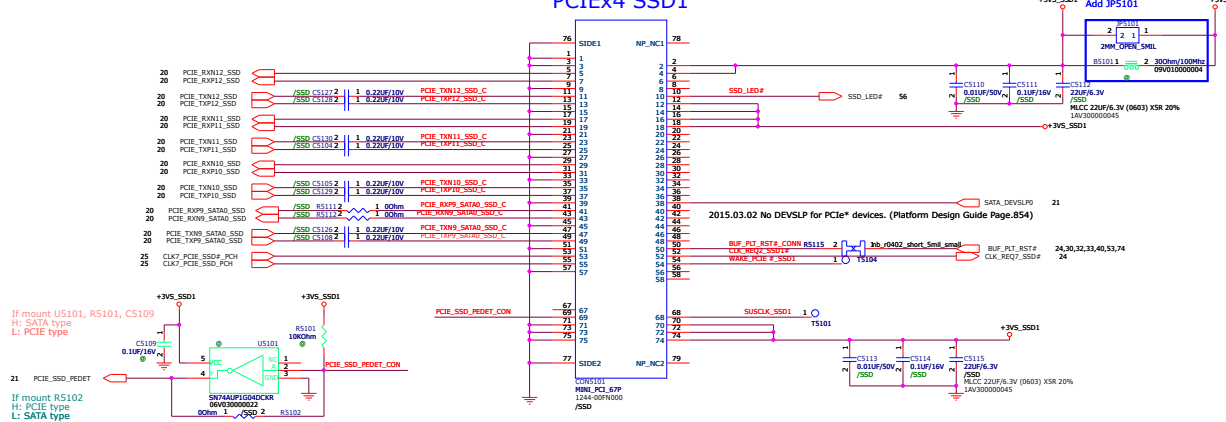


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

[illegible]

Table 5 – Standard SATA connector (3.5 inch &amp; 2.5 inch HDD)

	Name	Type	Description	Cable Usage # <sup>1</sup>	Backstop Usage # <sup>2</sup>
Signal Segment	S1	GN	Ground	1 <sup>1</sup> Male	2 <sup>2</sup> Male
	S2	A <sup>3</sup>	Differential Signal Pair A	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	S3	A <sup>3</sup>	Differential Signal Pair A	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	S4	B <sup>3</sup>	Differential Signal Pair B	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	S5	B <sup>3</sup>	Differential Signal Pair B	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	S6	GN	Ground	1 <sup>1</sup> Male	2 <sup>2</sup> Male
Power Feed	P1	REF	Reference Voltage	2 <sup>1</sup> Male	3 <sup>2</sup> Male
	P2	REF	Reference Voltage	2 <sup>1</sup> Male	3 <sup>2</sup> Male
	P3	DEVSUP	Device Supply	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	P4	DEVSUP	Device Supply	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	P5	GN	Ground	1 <sup>1</sup> Male	2 <sup>2</sup> Male
	P6	GN	Ground	1 <sup>1</sup> Male	2 <sup>2</sup> Male
	P7	V <sub>1</sub>	1 V Power Pre-charge	2 <sup>1</sup> Male	3 <sup>2</sup> Male
	P8	V <sub>1</sub>	1 V Power Pre-charge	2 <sup>1</sup> Male	3 <sup>2</sup> Male
	P9	V <sub>2</sub>	5 V Power	2 <sup>1</sup> Male	3 <sup>2</sup> Male
	P10	V <sub>2</sub>	5 V Power	2 <sup>1</sup> Male	3 <sup>2</sup> Male
Data Segment	D1	GN	Ground	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	D2	GN	Ground	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	D3	DATA	Device Activity Signal / Discrete Channel Select	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	D4	DATA	Device Activity Signal / Discrete Channel Select	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	D5	DATA	Device Activity Signal / Discrete Channel Select	2 <sup>1</sup> Male	2 <sup>2</sup> Male
	D6	DATA	Device Activity Signal / Discrete Channel Select	2 <sup>1</sup> Male	2 <sup>2</sup> Male
Control Segment	C1	GN	Ground	1 <sup>1</sup> Male	1 <sup>2</sup> Male
	C2	GN	Ground	1 <sup>1</sup> Male	1 <sup>2</sup> Male
	C3	V <sub>1</sub>	1 V Power Pre-charge	2 <sup>1</sup> Male	3 <sup>2</sup> Male
	C4	V <sub>1</sub>	1 V Power Pre-charge	2 <sup>1</sup> Male	3 <sup>2</sup> Male
	C5	V <sub>2</sub>	5 V Power	2 <sup>1</sup> Male	3 <sup>2</sup> Male
	C6	V <sub>2</sub>	5 V Power	2 <sup>1</sup> Male	3 <sup>2</sup> Male

For specific optional usage see pin 19 (see § 6.1.3).

<sup>1</sup> Although the male order is shown, it is not supported in conjunction with the cable connector receptacles.

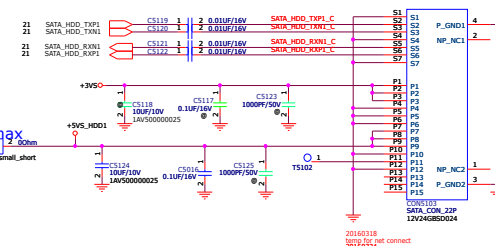
<sup>2</sup> All cable sequences assume zero angular offset between connectors.

<sup>3</sup> A<sup>3</sup> and B<sup>3</sup> indicate sequences assume 20 pin angular offset between connectors.

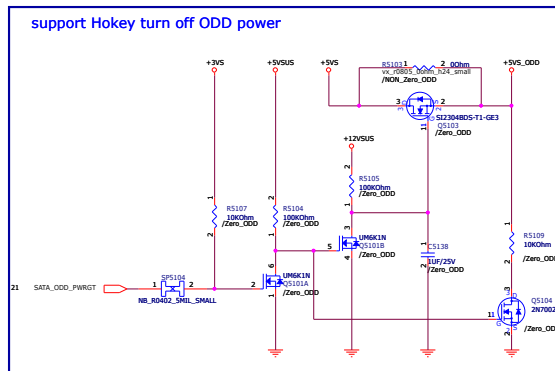
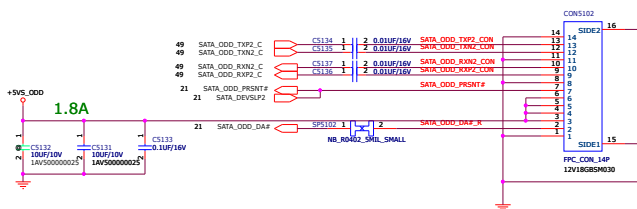
<sup>4</sup> Previous versions of the specification assigned 3,3 V to pins P1, P2 and P3. In addition, device activity signal D1, D2, D3 and D4 were assigned to pins P1, P2, P3 and P4.

<sup>5</sup> It is recommended to have P1 and C1 connected together for the purpose of signal functionality.

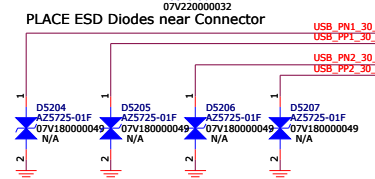
SATA HDD



## SATA ODD







# NGFF 2230 Key A\_slot A(WIFI)

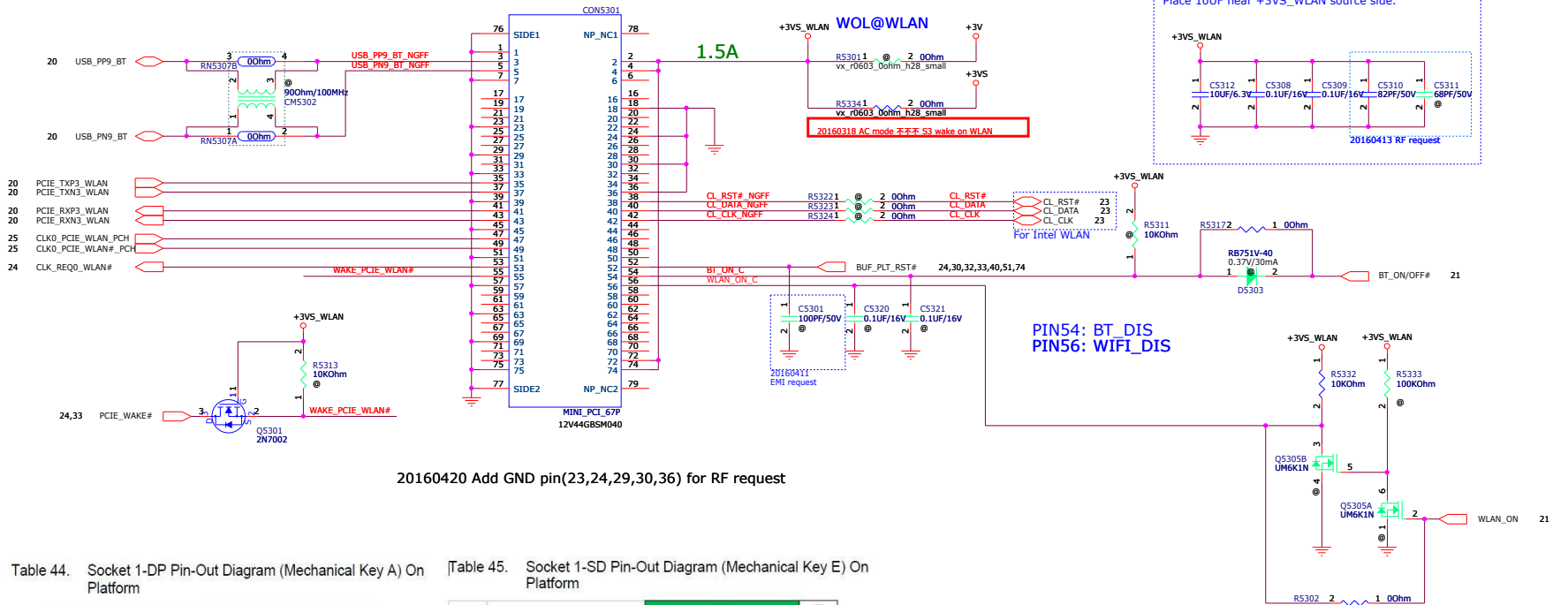
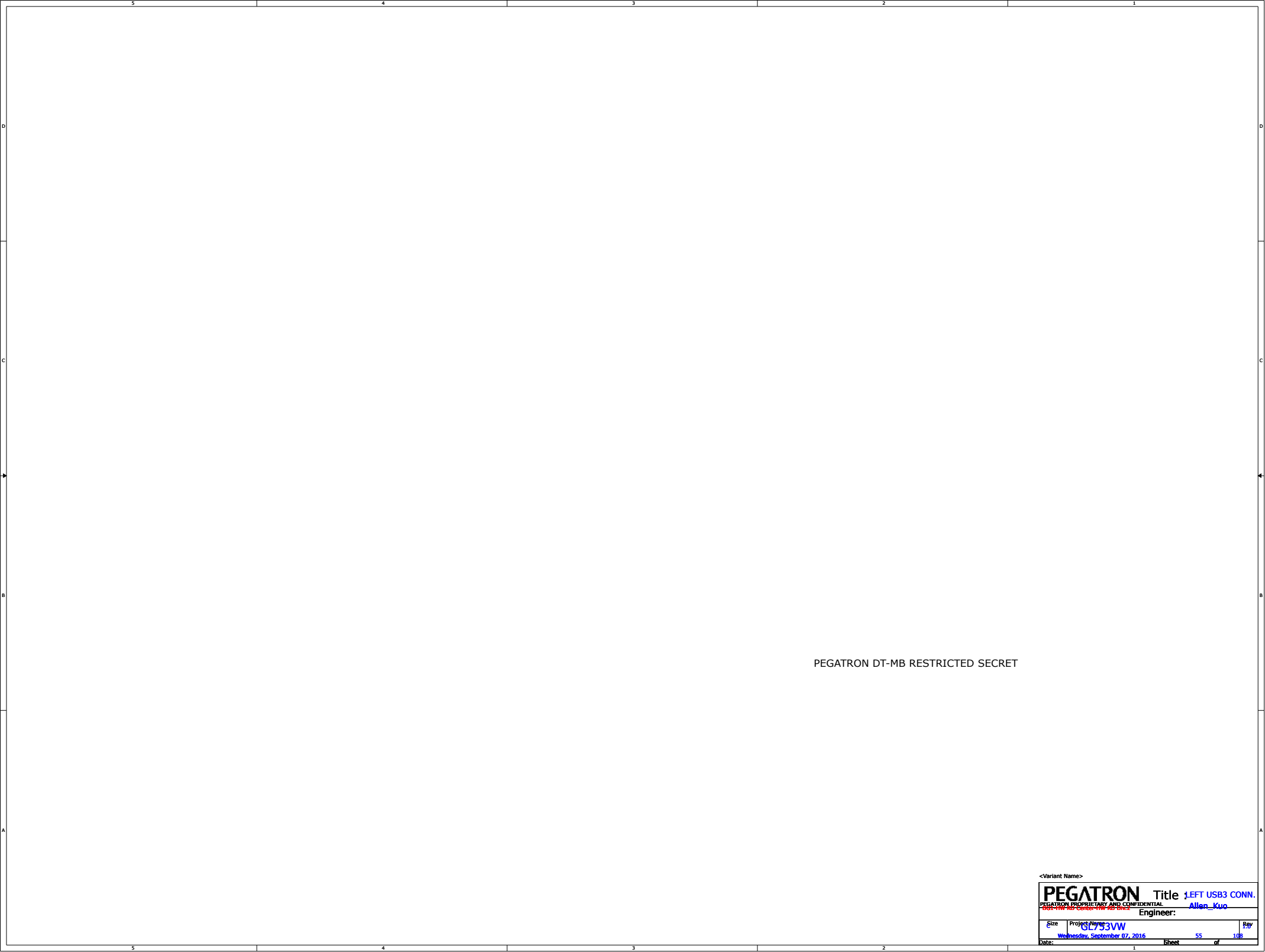


Table 44. Socket 1-DP Pin-Out Diagram (Mechanical Key A) On Platform

74	3.3V	GND	75
72	3.3V	REFCLKn1	73
70	PEWAKE1# (I/O)(0/3.3V)	REFCLKp1	71
68	CLKREQ1# (I/O)(0/3.3V)	GND	69
66	PERST1# (O)(0/3.3V)	PERn1	67
64	RESERVED	PERp1	65
62	ALERT# (I)(0/3.3V)	GND	61
60	I2C_CLK (O)(0/3.3V)	PETn1	63
58	I2C_DATA (O)(0/3.3V)	PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK1(32KHz) (O)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKn0	49
46	COEX2(I/O)(0/1.8V)	REFCLKp0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	GND	PETn0	37
34	DP_MLdp	PETp0	35
32	DP_MLn	GND	33
30	GND	DP_HPD (I/O)(0/3.3V)	31
28	DP_MLdp	DP_MLdp	29
26	DP_MLn	DP_MLn	27
24	GND	DP_MLdp	25
22	DP_AUXp	DP_MLdp	23
20	DP_AUXn	DP_MLn	21
18	GND	MLDIR Sense (I)	19
16	LED2# (I)(OD)	GND	17
14	Connector Key	Connector Key	15
12	Connector Key	Connector Key	13
10	Connector Key	Connector Key	11
8	Connector Key	Connector Key	9
6	LED1# (I)(OD)	GND	7
4	3.3V	USB_D+	5
2	3.3V	USB_D-	3
		GND	1

Table 45. Socket 1-SD Pin-Out Diagram (Mechanical Key E) On Platform

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SINK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PERn1	67
64	RESERVED	RESERVED/PERp1	65
62	ALERT# (I)(0/3.3V)	GND	63
60	I2C_CLK (O)(0/3.3V)	RESERVED/PETn1	61
58	I2C_DATA (O)(0/3.3V)	RESERVED/PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK1(32KHz) (O)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKn0	49
46	COEX2(I/O)(0/1.8V)	REFCLKp0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0/1.8V)	PETn0	37
34	UART CTS (I)(0/1.8V)	PETp0	35
32	UART TXD (O)(0/1.8V)	GND	33
30	Connector Key	Connector Key	31
28	Connector Key	Connector Key	29
26	Connector Key	Connector Key	27
24	Connector Key	Connector Key	25
22	UART RXD (I)(0/1.8V)	SDIO RESET# (O)(0/1.8V)	23
20	UART WAKE# (I)(0/3.3V)	SDIO WAKE# (I)(0/1.8V)	21
18	GND	SDIO DATA3 (I/O)(0/1.8V)	19
16	LED2# (I)(OD)	SDIO DATA2 (I/O)(0/1.8V)	17
14	PCM_OUT/125 SD_OUT (O)(0/1.8V)	SDIO DATA1 (I/O)(0/1.8V)	15
12	PCM_IN/125 SD_IN (I)(0/1.8V)	SDIO DATA0 (I/O)(0/1.8V)	13
10	PCM_SYNC/125 WS (O)(0/1.8V)	SDIO CMD0 (I/O)(0/1.8V)	11
8	PCM_CLK/125 SCK (O)(0/1.8V)	SDIO CLK (O)(0/1.8V)	9
6	LED1# (I)(OD)	GND	7
4	3.3V	USB_D+	5
2	3.3V	USB_D-	3
		GND	1

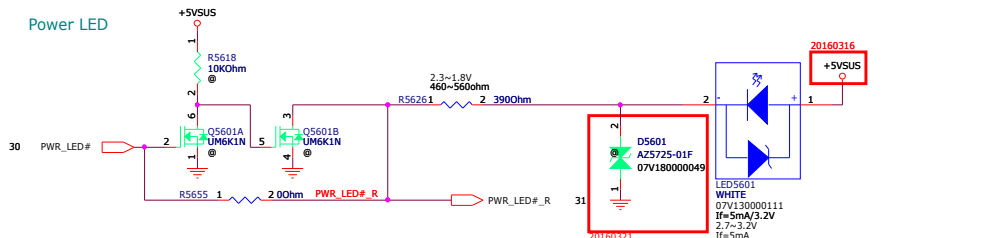


PEGATRON DT-MB RESTRICTED SECRET

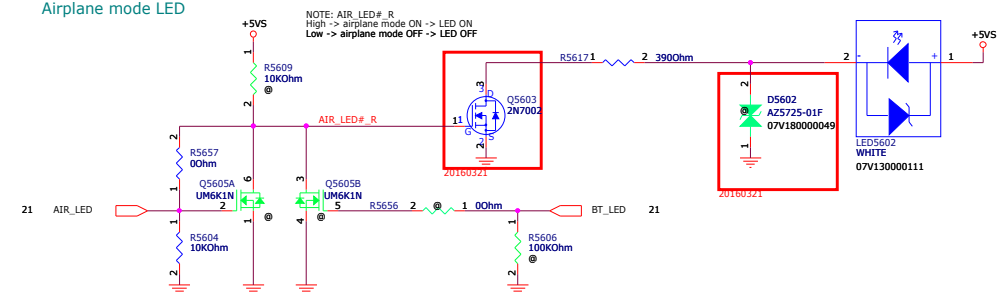
<Variant Name>

<b>PEGATRON</b>		Title	
<small>PEGATRON PROPRIETARY AND CONFIDENTIAL <del>DT-MB RESTRICTED SECRET</del></small>		LEFT USB3 CONN.	
		Engineer: Allen_Kuo	
Size	Project Name		Rev
	GL753VW		001
Date:	Wednesday, September 07, 2016	Sheet	55 of 108

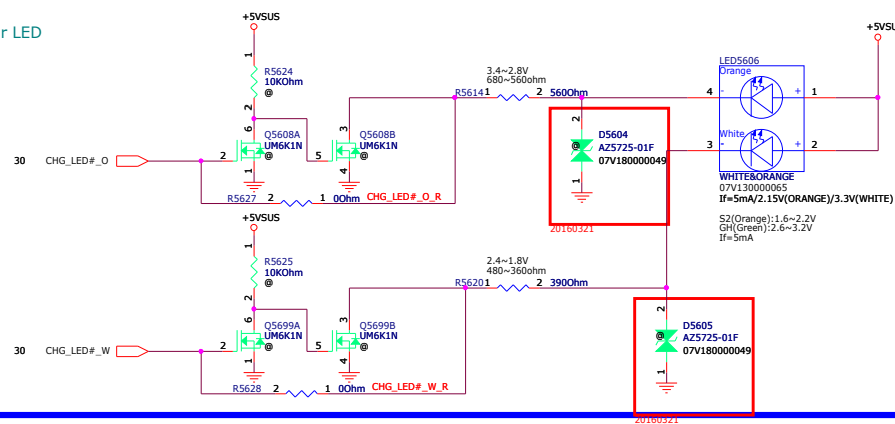
## Power LED



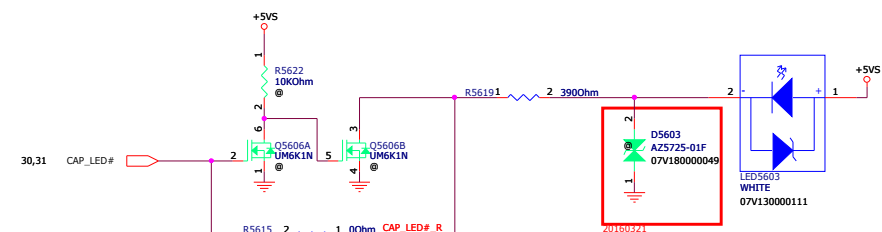
## Airplane mode LED



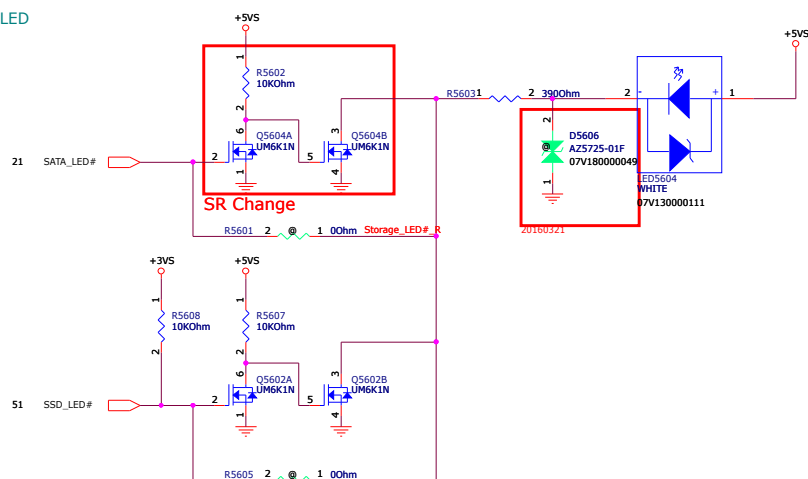
## Charger LED



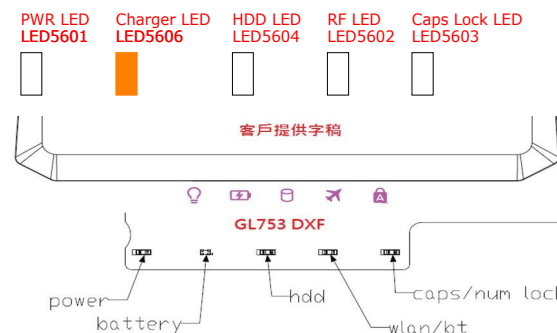
## Caps Lock LED



## HDD LED



## MB LED Placement Left-->Right



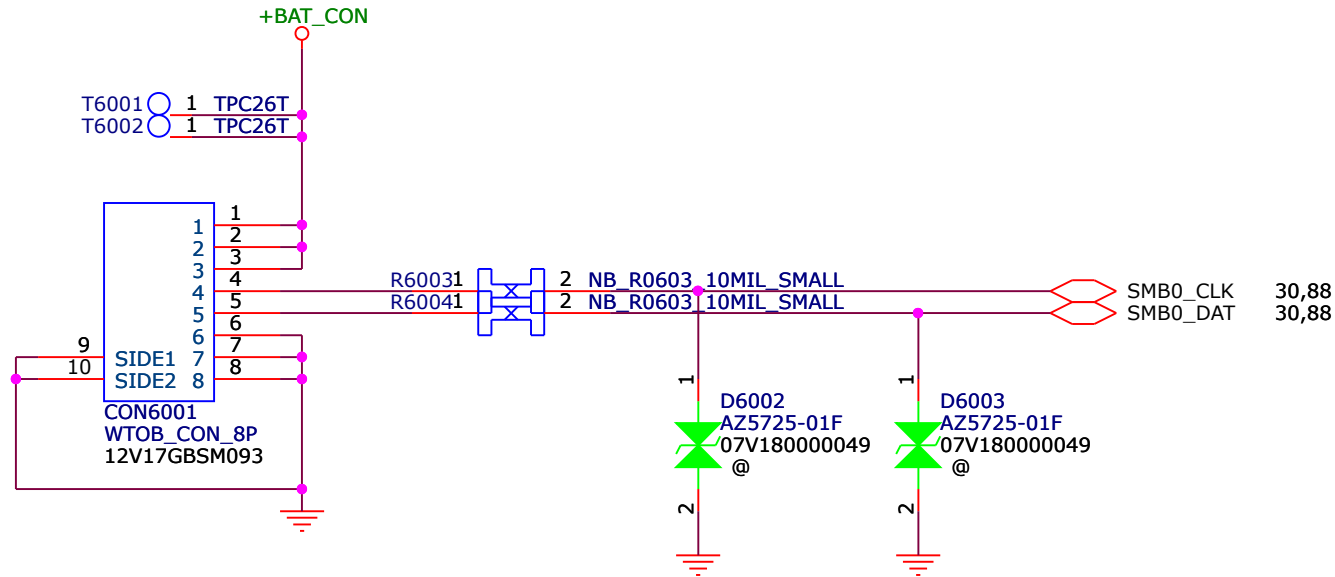
<Variant Name>



# 60.BATT CON/AC IN

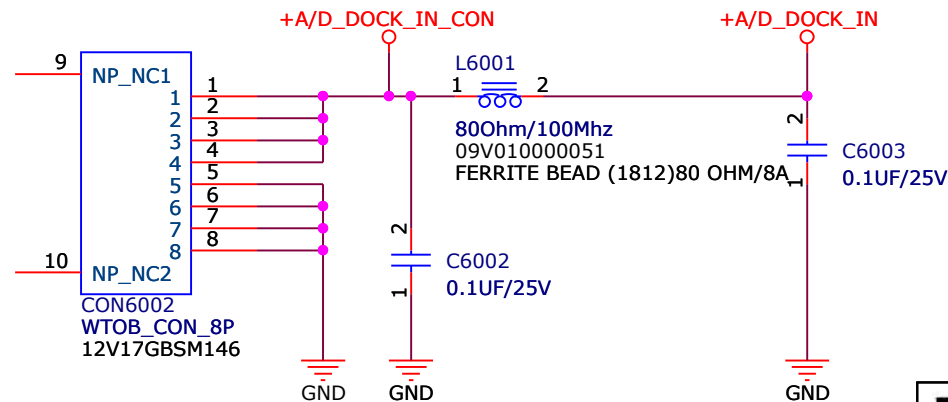
## BATTERY CONNECTOR

Battery  
PIN 1: Pack+  
PIN 2: Pack+  
PIN 3: Pack+  
PIN 4: SMBus Clock  
PIN 5: SMBus Data  
PIN 6: Pack-  
PIN 7: Pack-  
PIN 8: Pack-



## AC IN CONNECTOR

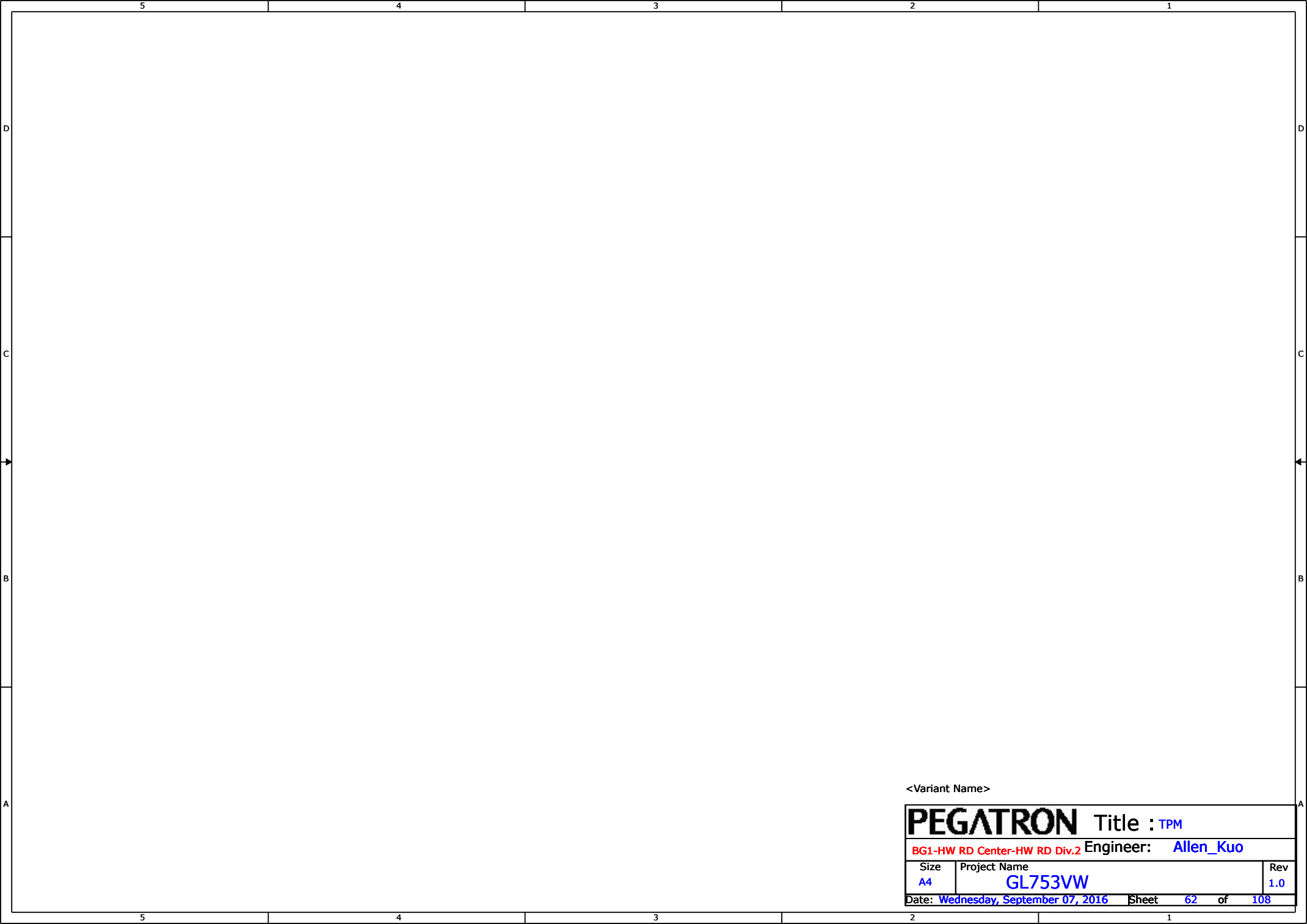
Adaptor  
120W



<b>PEGATRON</b>		Title: <b>BATT CON/AC IN</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Size: <b>A</b>		Engineer: <b>Allen_Kuo</b>	
Project Name: <b>GL733VW</b>		Rev: <b>1.0</b>	
Date: <b>Wednesday, September 07, 2016</b>		Sheet <b>60</b> of <b>108</b>	





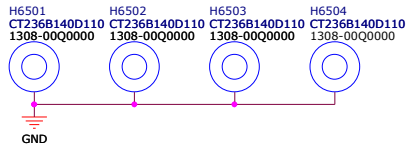


<Variant Name>

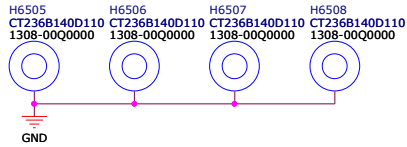
<b>PEGATRON</b>		Title : <b>TPM</b>	
<b>BG1-HW RD Center-HW RD Div.2</b>		Engineer: <b>Allen_Kuo</b>	
Size <b>A4</b>	Project Name <b>GL753VW</b>		Rev <b>1.0</b>
Date: <b>Wednesday, September 07, 2016</b>		Sheet	<b>62</b> of <b>108</b>

## 65.NUT,Screw hole,Tooling hole

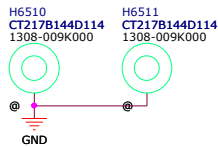
## CPU NUT



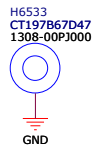
# GPU NUT



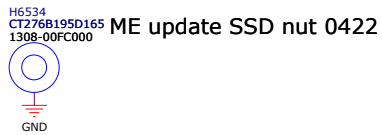
# PCH NUT



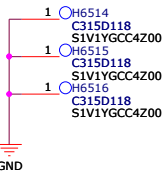
## Hall Sensor Brd NUT



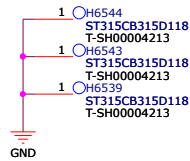
## SSD NUT



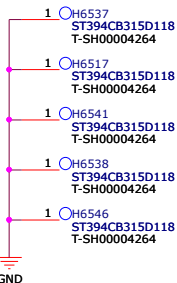
TOP: phi 8 drill 3  
BOT: phi 8 drill 3



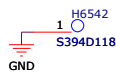
TOP: Square 8 drill 3  
BOT: phi 8 drill 3



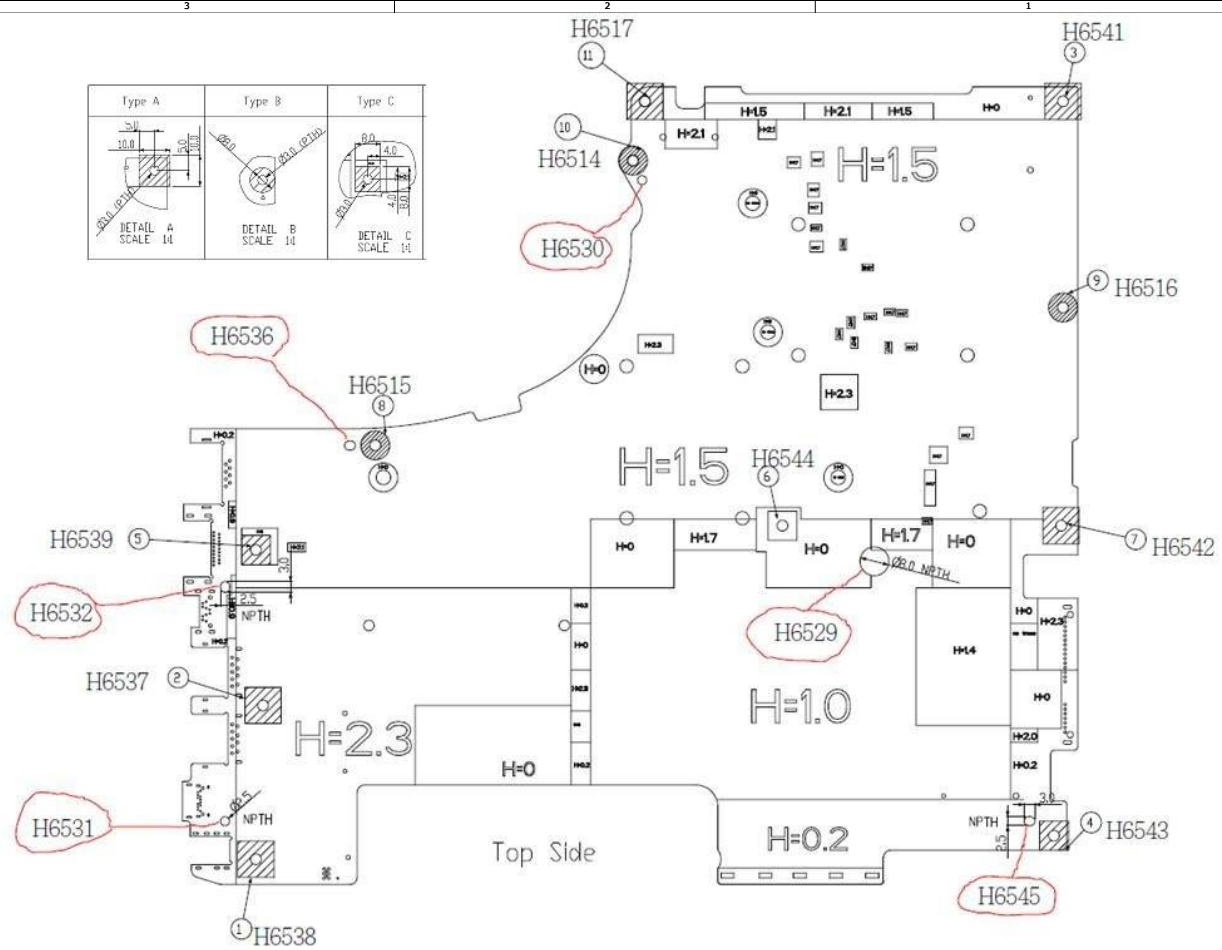
TOP: Square 10 drill 3  
BOT: phi 8 drill 3



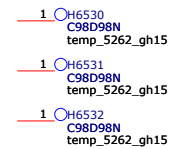
TOP: Square 10 drill 3  
BOT: Square 10 drill 3



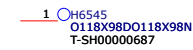
Type A	Type B	Type C
<p>DETAIL A SCALE 1:1</p>	<p>DETAIL B SCALE 1:1</p>	<p>DETAIL C SCALE 1:1</p>



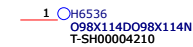
NPTH\_2.5phi



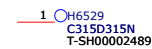
NPTH\_2.5 x 3 phi



NPTH\_2.5 x 2.9 phi



NPTH\_8phi

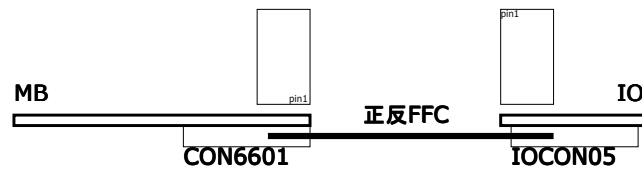


<Variant Name>

**PEGATRON** Title: Screw hole  
PEGATRON PROPRIETARY AND CONFIDENTIAL Allen\_Kuo  
BG1-11W-RD-Center-11W-RD-Div.2 Engineer:

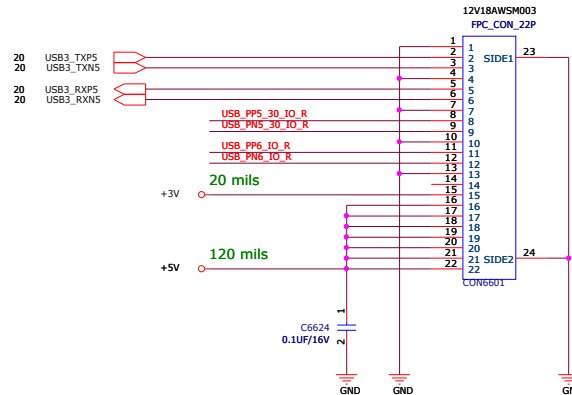
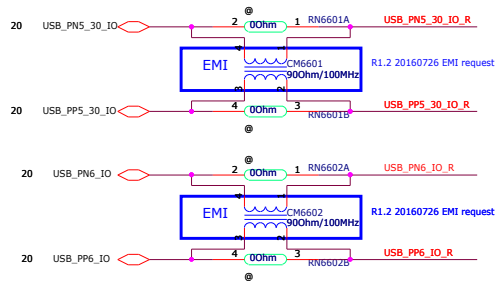
Size	Project Name	Rev
Custom	GL753VW	1.0
Date: Wednesday, September 07, 2016		Sheet 65 of 108

# IO BD CONN. (MB SIDE)



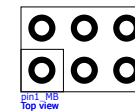
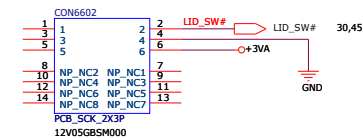
+3V	24,45,53,57,68,91
+3VA	25,30,31,57,74,81,88,91,93
+5V	7,12,52,57,91

Need check pin define

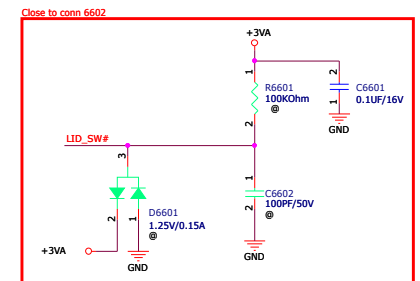
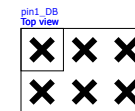


## MB Side USB Re-driver (move to IO\_BD side)

## Hall sensor Conn. (MB SIDE)



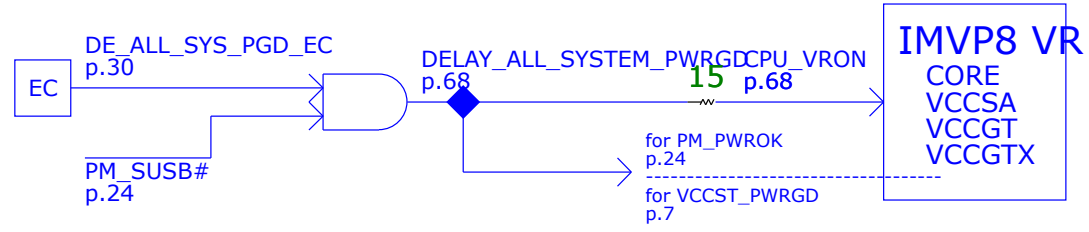
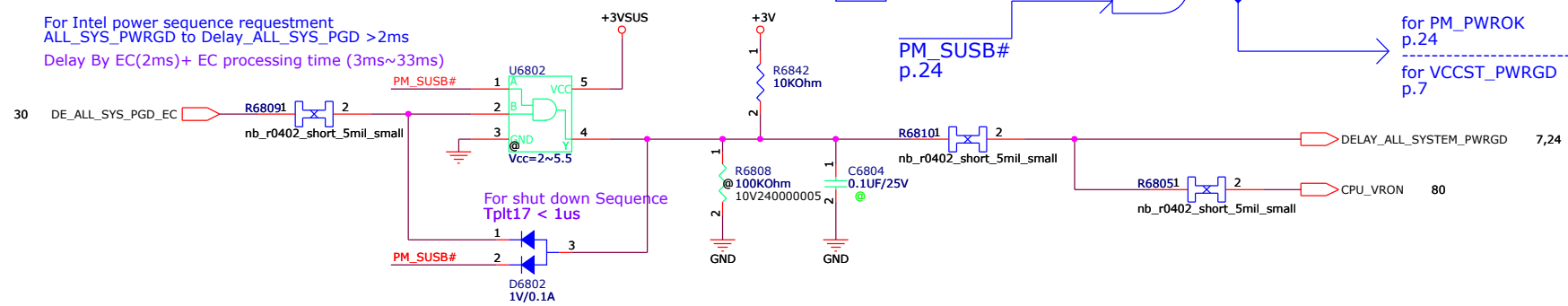
CON6602 LID01  
pin2:LID\_SW# pin3:LID\_SW#\_H  
pin4:GND pin5:GND\_H  
pin6:+3VA pin7:+3VA\_H



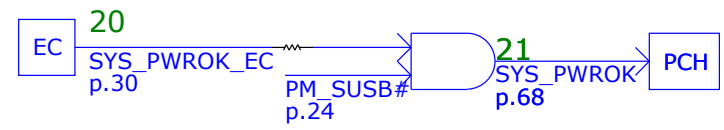
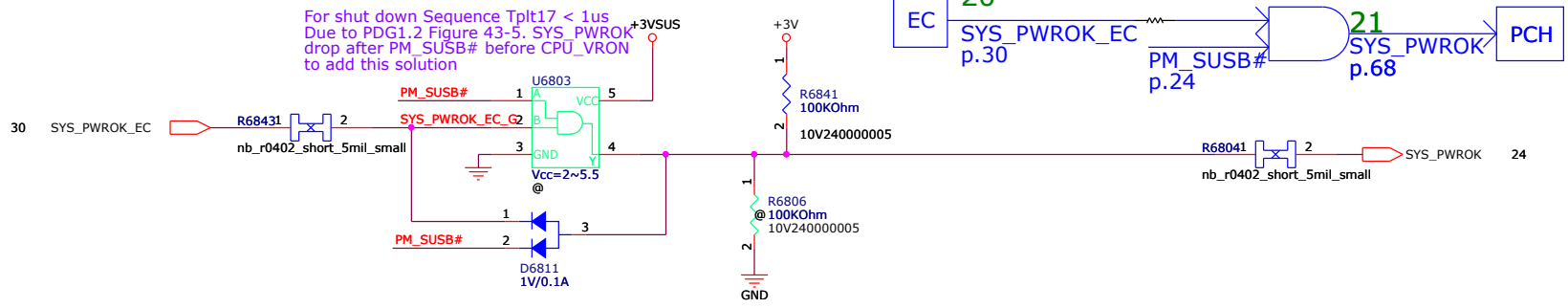
EC processing time (3ms~33ms)



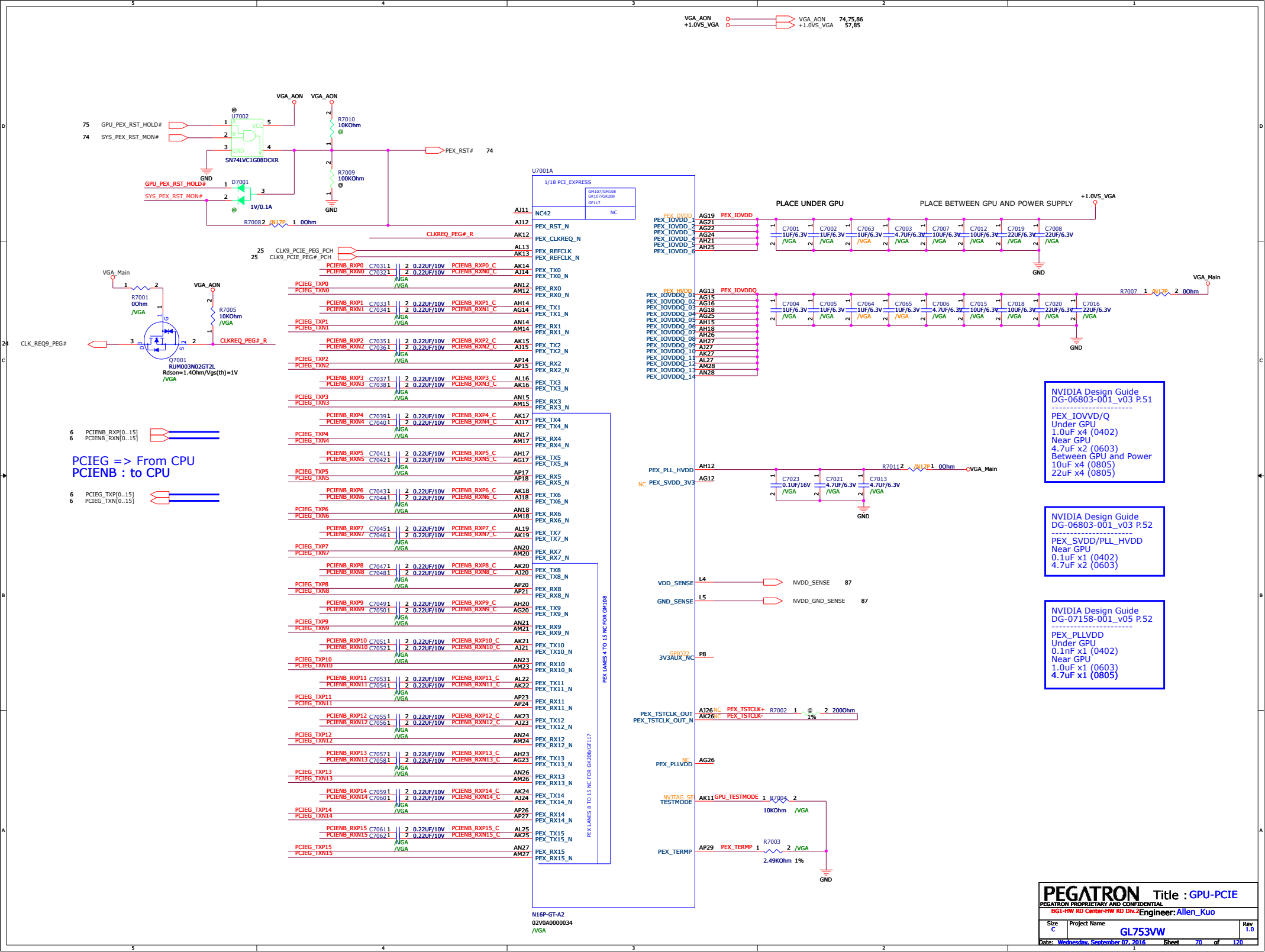
For Intel power sequence requestment  
ALL\_SYS\_PWRGD to Delay\_ALL\_SYS\_PGD >2ms  
Delay By EC(2ms)+ EC processing time (3ms~33ms)



For shut down Sequence Tplt17 < 1us  
Due to PDG1.2 Figure 43-5. SYS\_PWROK  
drop after PM\_SUSB# before CPU\_VRON  
to add this solution



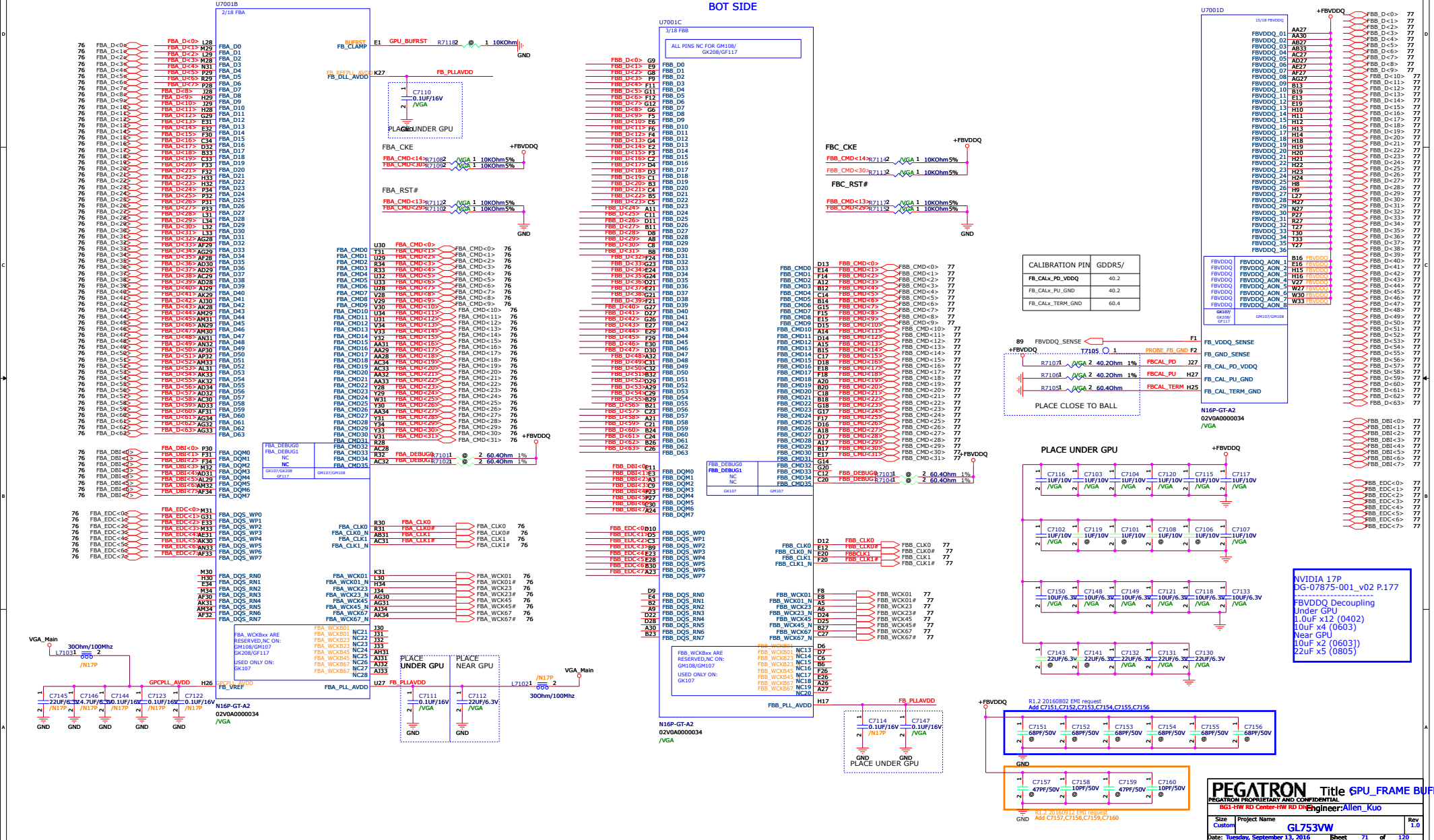
delay by EC, delay circuit no longer needed





## BOT SIDE

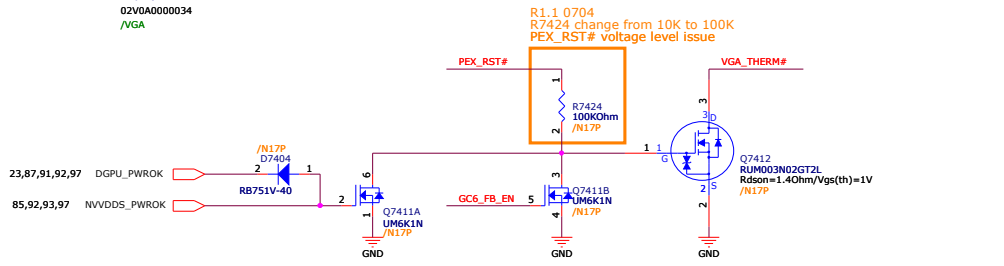
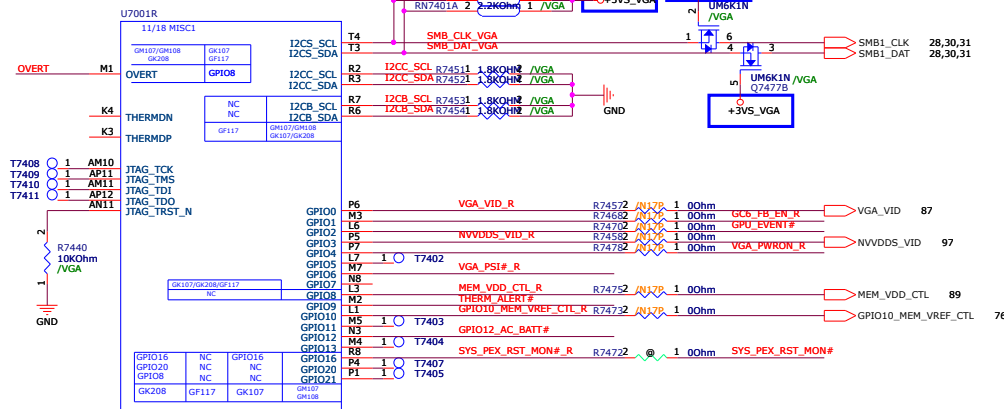
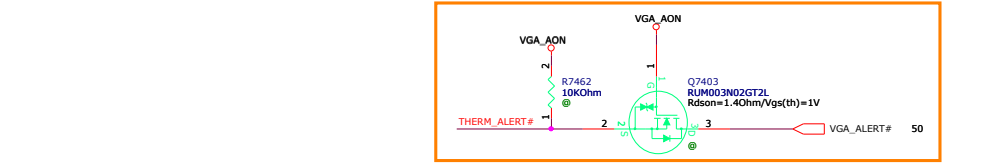
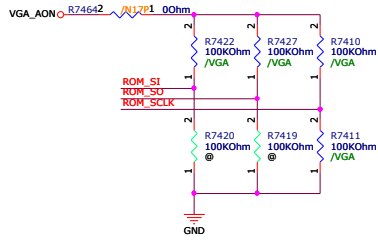
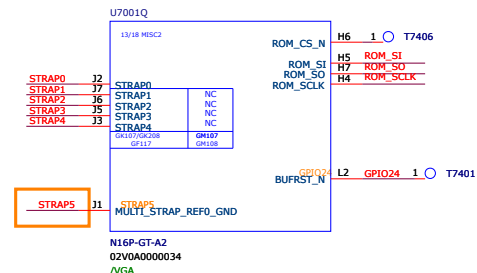
## BOT SIDE



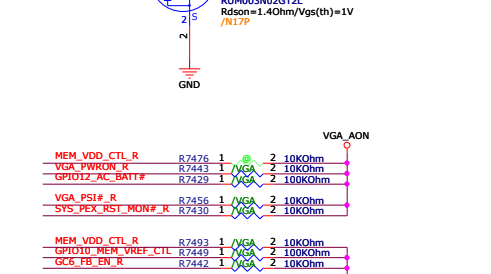
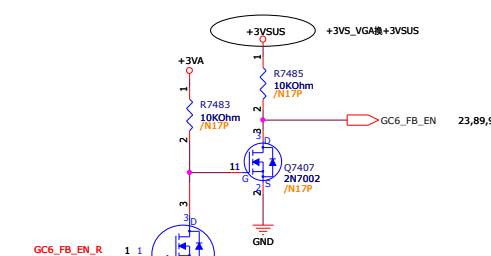
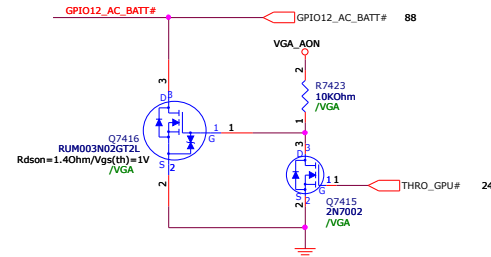
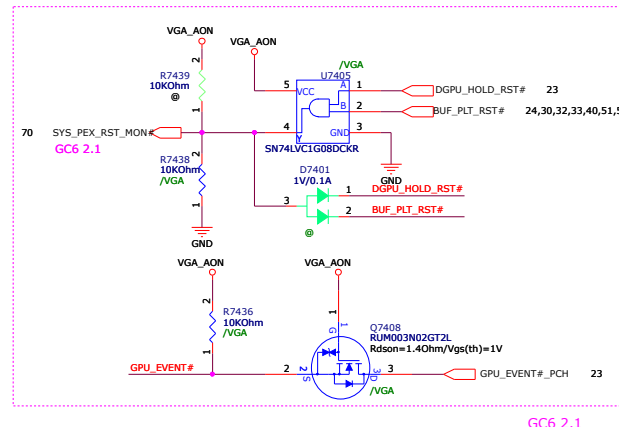
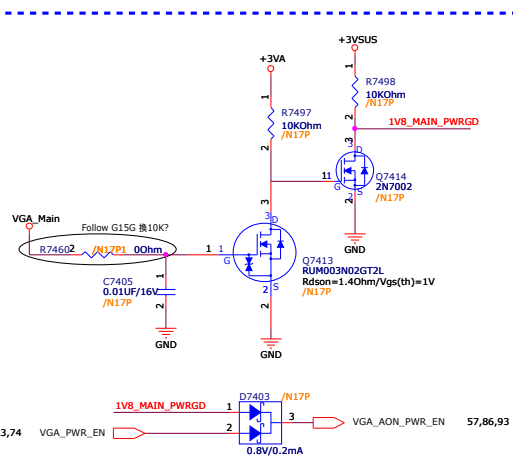
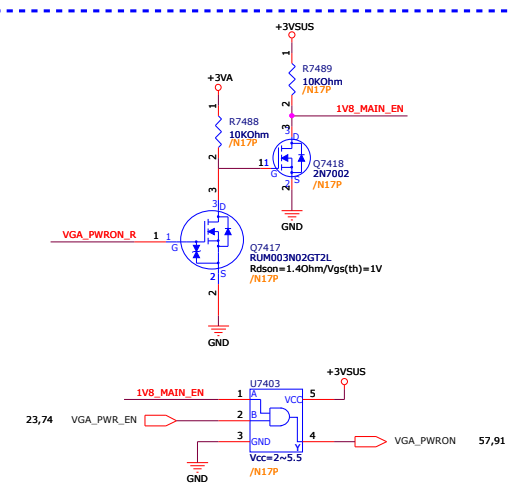
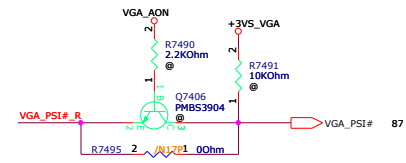
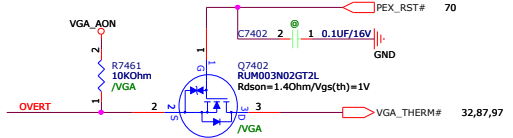


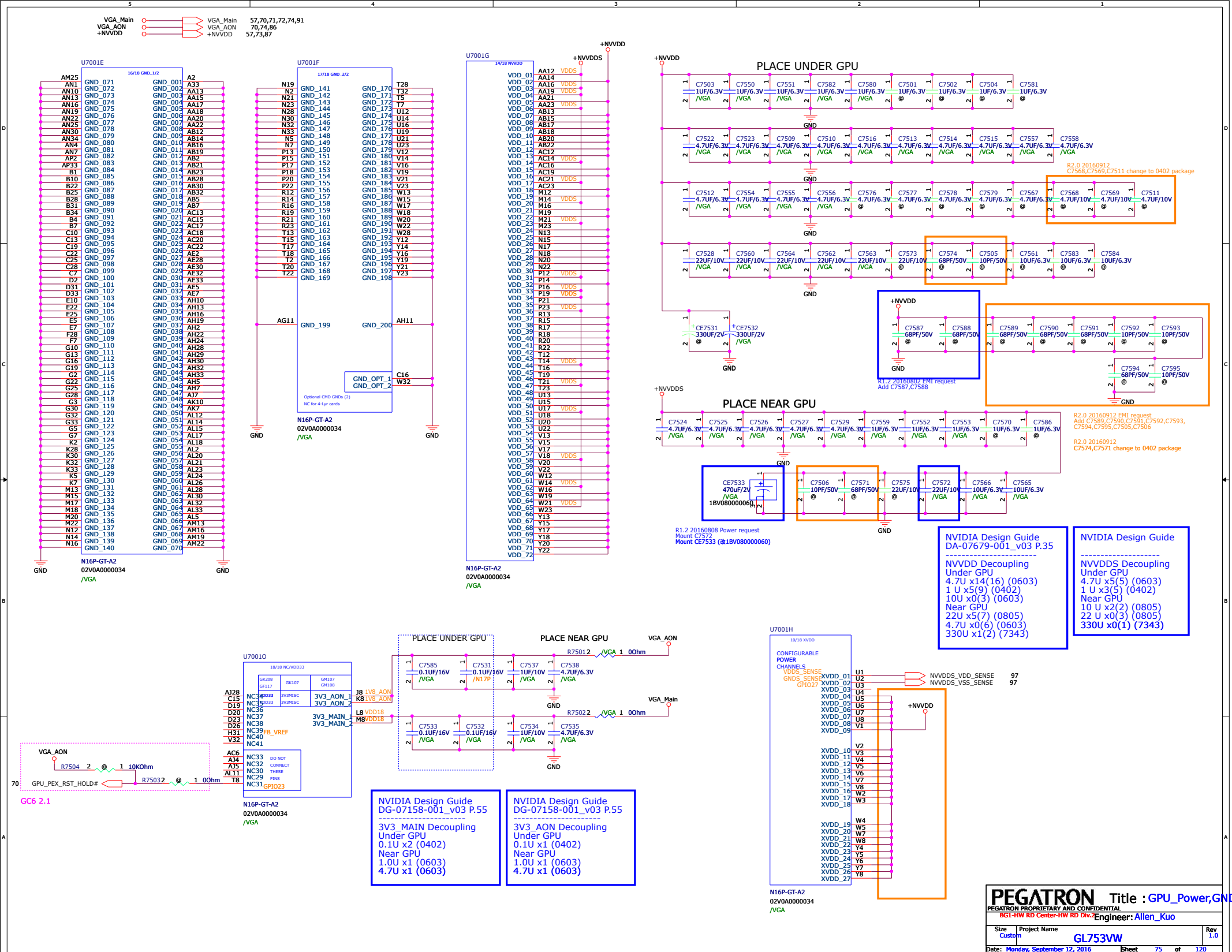






VGA\_Main 57,70,71,72,75,91  
VGA\_AON 70,75,86

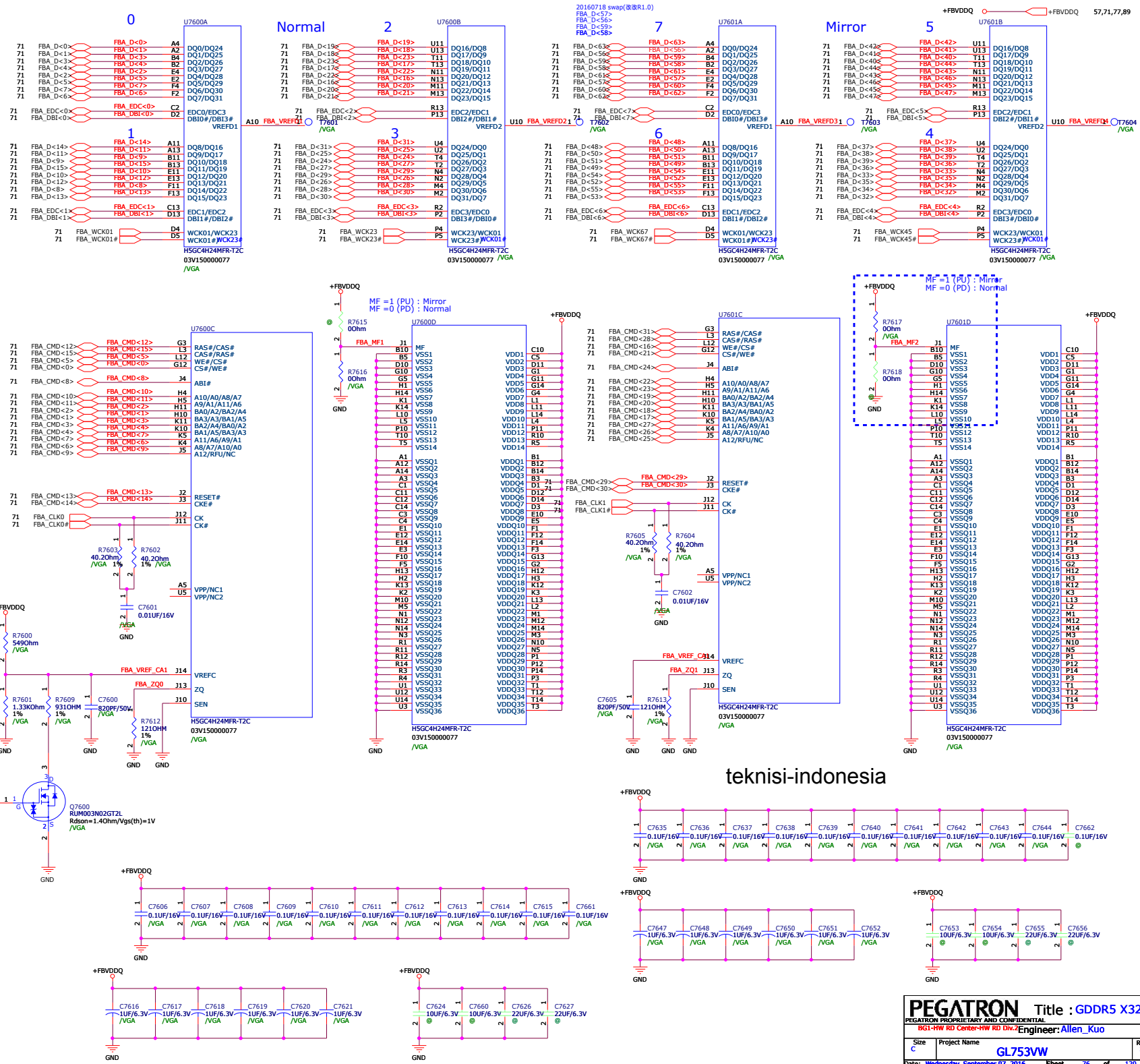




MEMORY : FBA Partition 31:0 (Normal)  
MEMORY : FBA Partition 63:32 (Mirror)

# GDDR5 Mode H Mapping

GB2B-64		GB2B-64	
GB4B-128	Ch0 0..31	GB4B-128	Ch1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3 BA3	CMD17	A3 BA3
CMD2	A2 BA0	CMD18	A2 BA0
CMD3	A4 BA2	CMD19	A4 BA2
CMD4	A5 BA1	CMD20	A5 BA1
CMD5	WE*	CMD21	WE*
CMD6	A7 A8	CMD22	A7 A8
CMD7	A6 A11	CMD23	A6 A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12 RFU	CMD25	A12 RFU
CMD10	A0 A10	CMD26	A0 A10
CMD11	A1 A9	CMD27	A1 A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

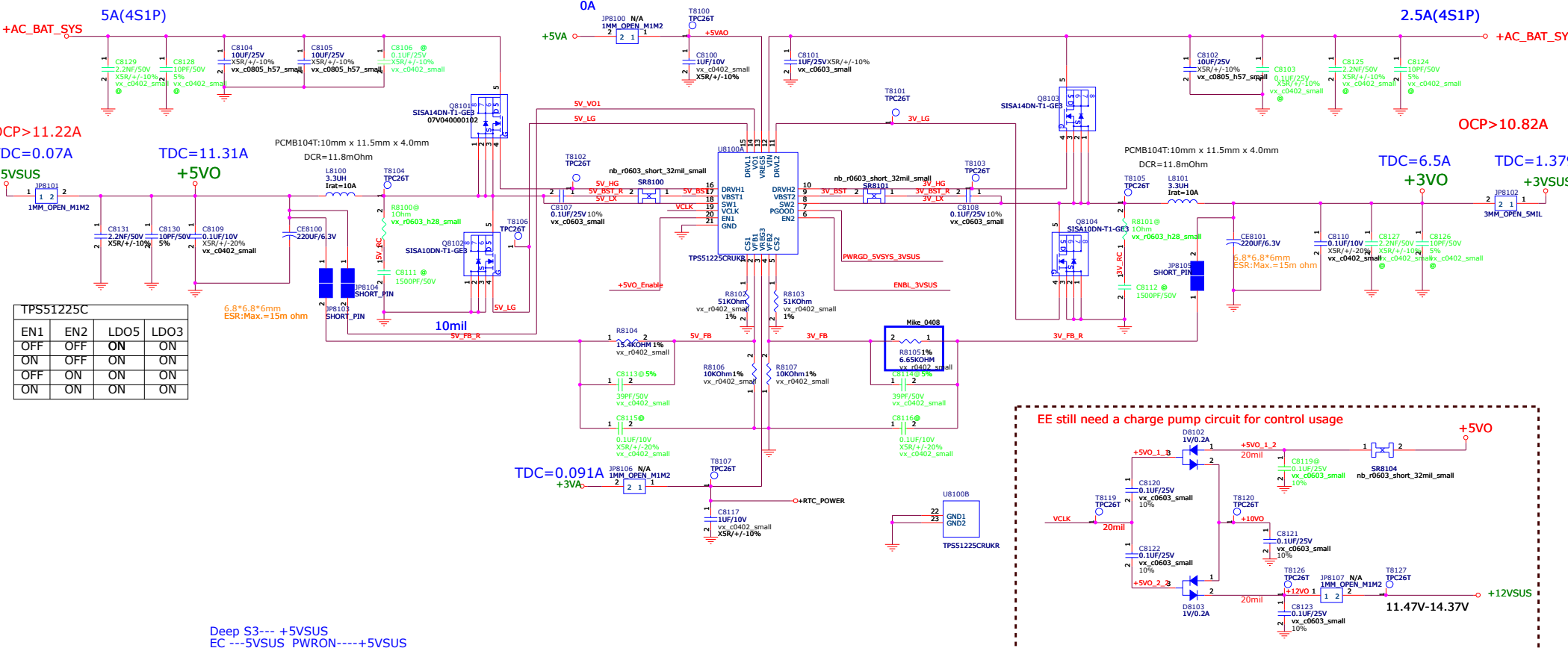


teknisi-indonesia

## GDDR5 Mode H Mapping

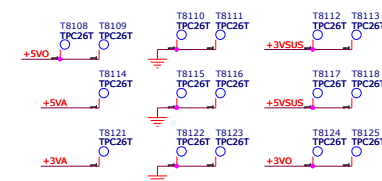
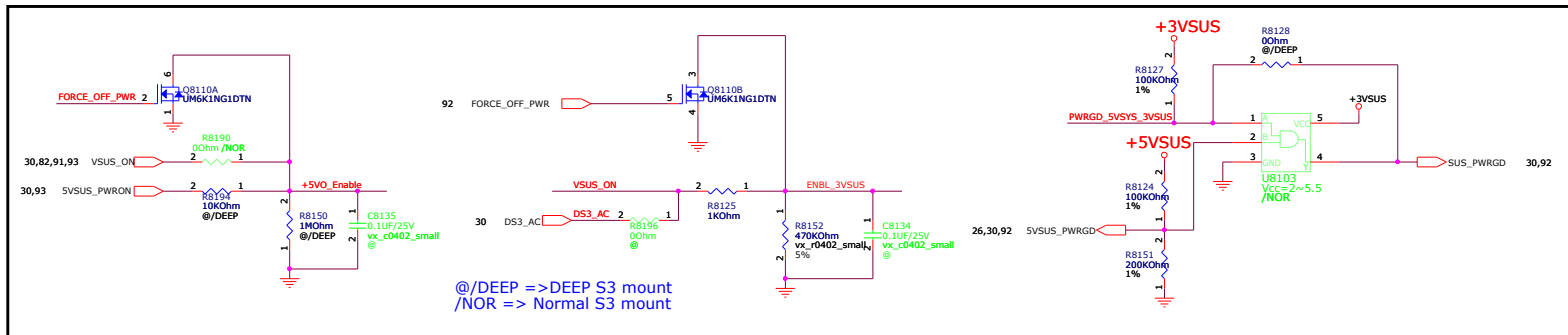


## +5VO & +3VO POWER SUPPLY



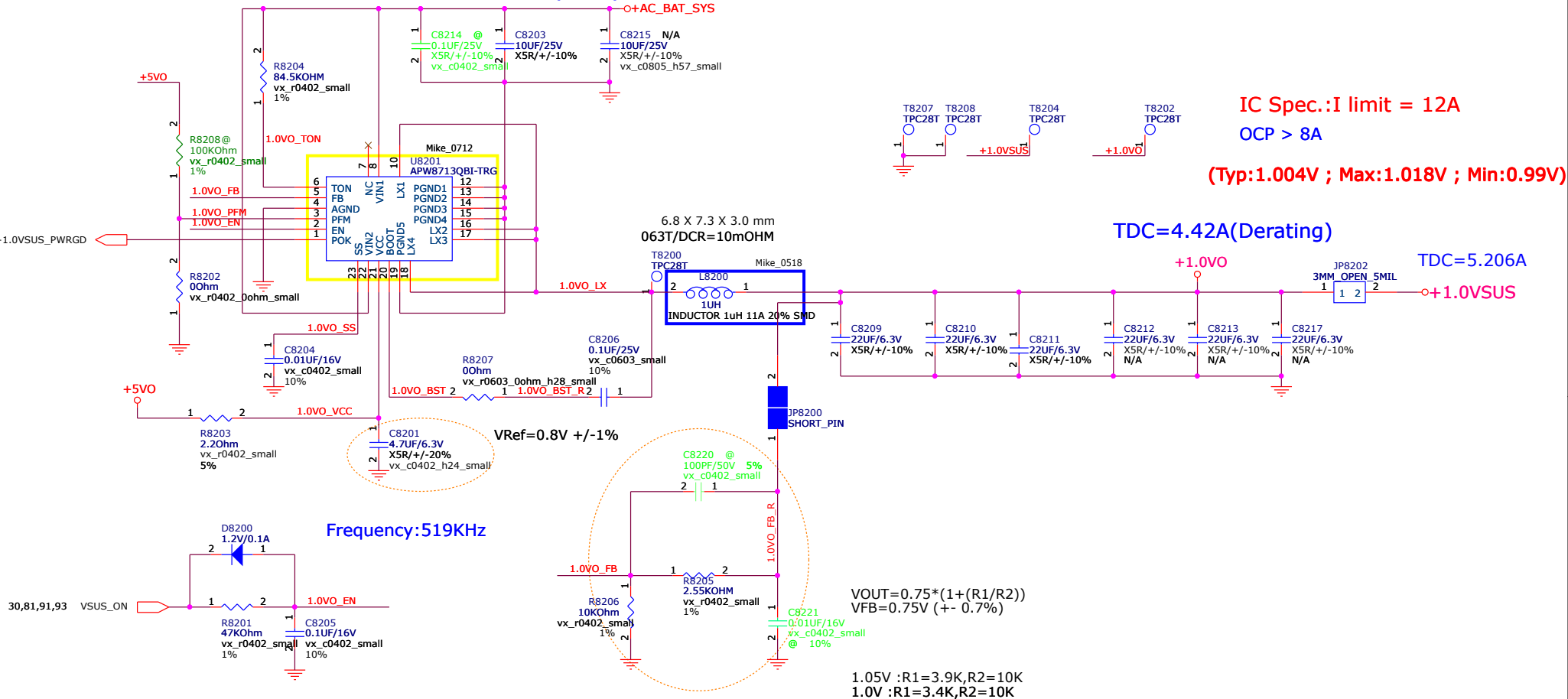
Deep S3--- +5VSUS  
EC ---5VSUS\_PWRON----+5VSUS  
This instant +3VSUS OFF  
Normal S3 4se VSUS ON ----3&5V

### ABBA Rule

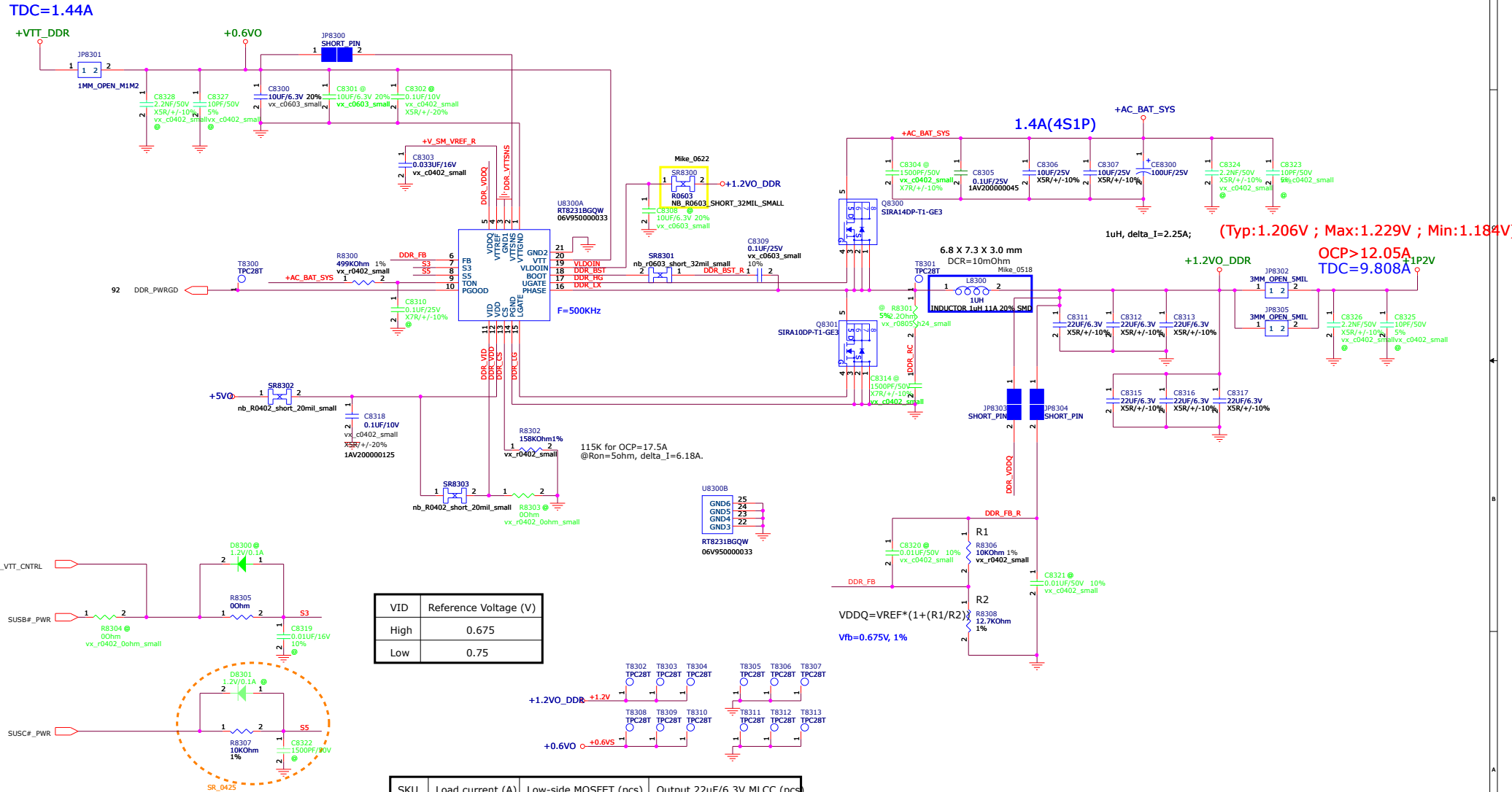


# 1.0VSUS POWER SUPPLY

0.92A(4S1P)



## DDR & VTT POWER SUPPLY

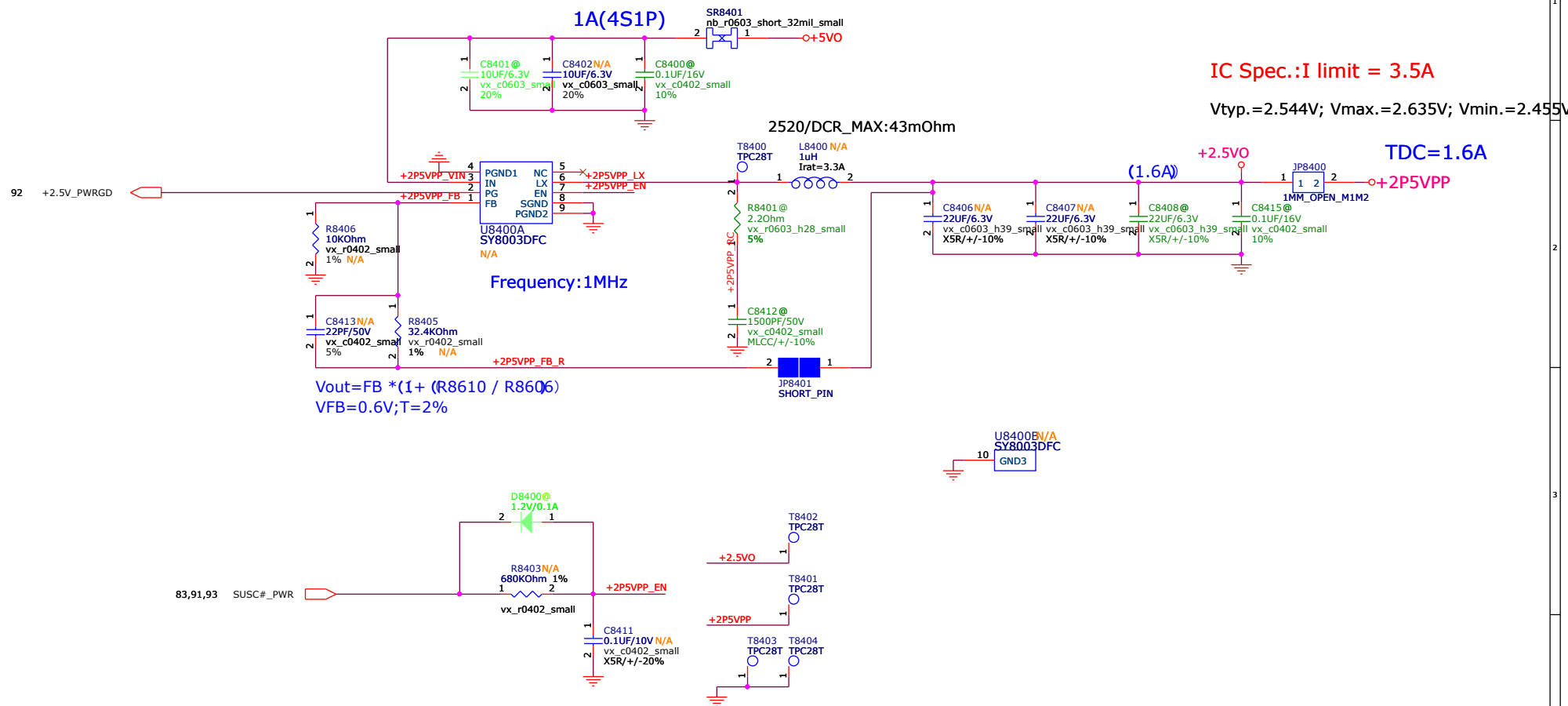


VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5



## +2.5V POWER SUPPLY



# 1.0VS\_VGA(+1P0V\_GPU) POWER SUPPLY

R8503 need to change Voltage 1V & 1.05V

+1.0VS\_VGA

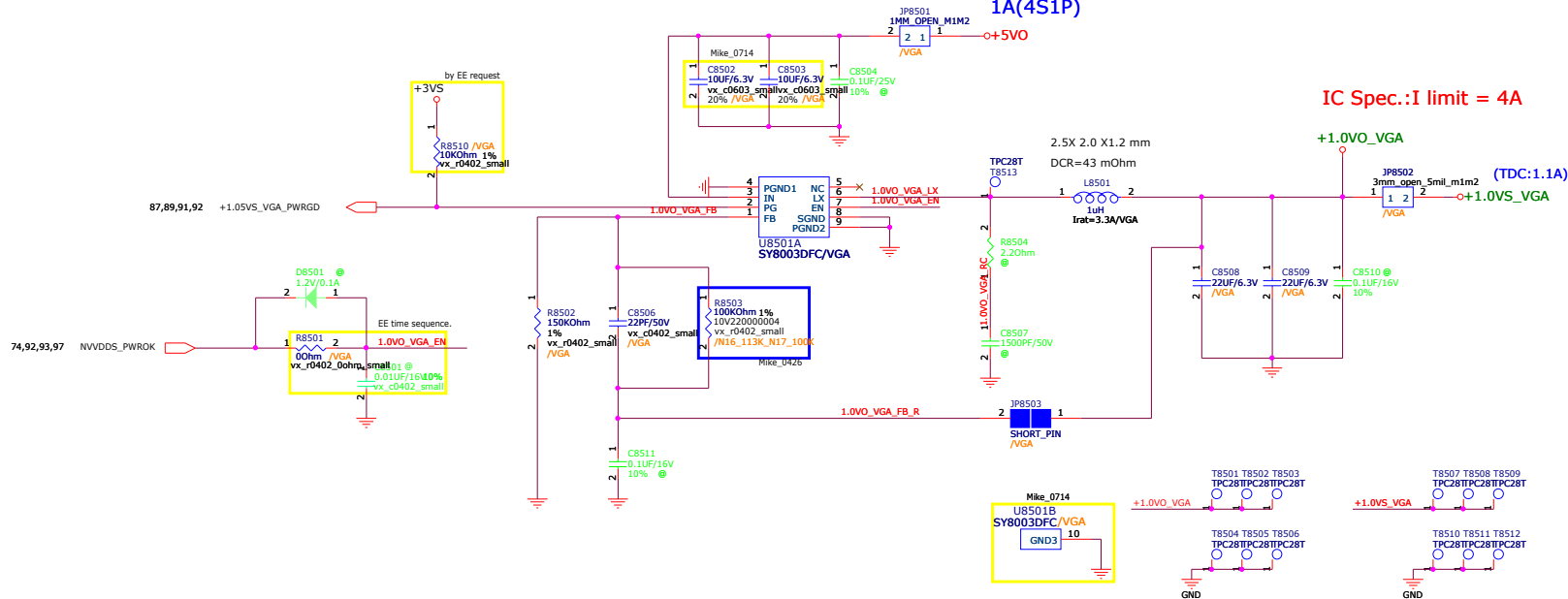
	N16P-GX	N17P-G1
EDP	2.9A	TBD
TDC	2.57A	3A
Voltage	1.05V	1V

R8503=113K-->Vtyp.=1.052V; Vmax.=1.077V; Vmin.=1.027V

R8503=100K-->Vtyp.=1V; Vmax.=1.023V; Vmin.=0.977V

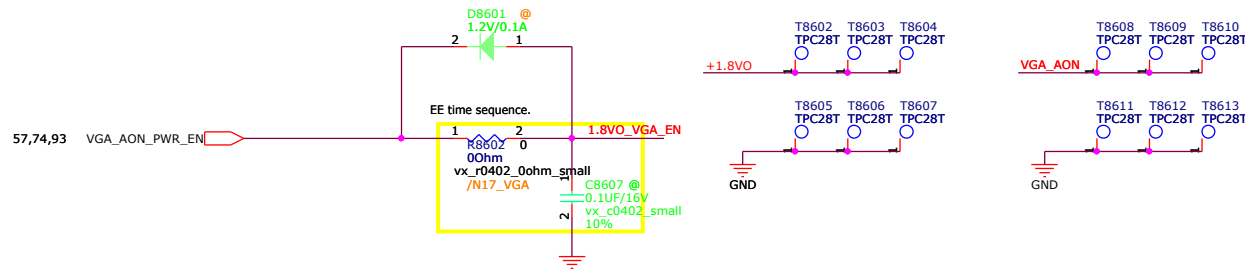
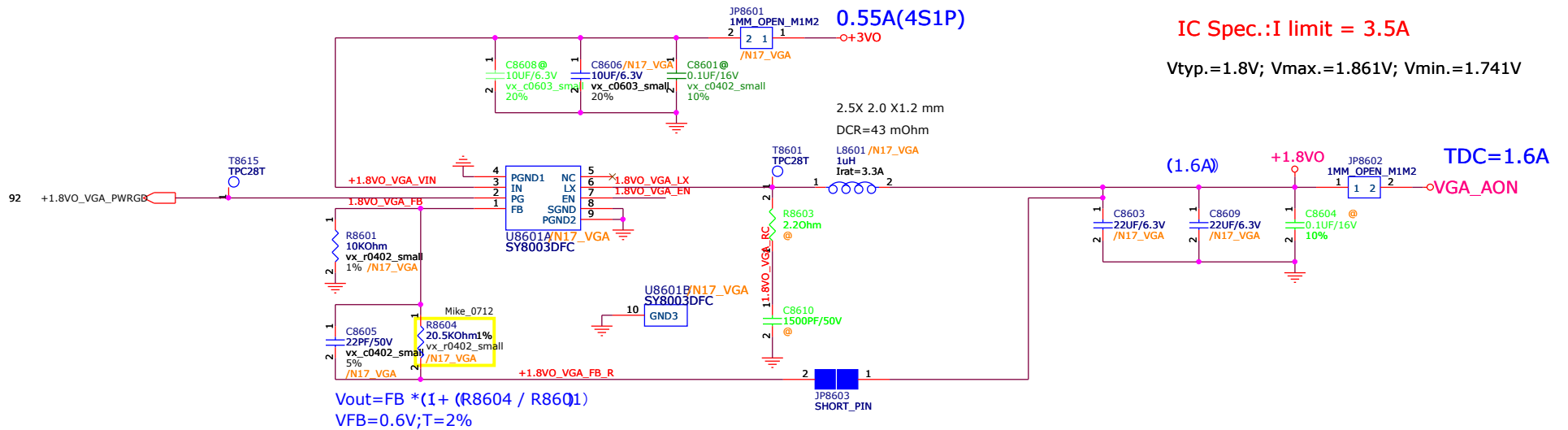
1A(4S1P)

IC Spec.: I limit = 4A



N16P-GX-->VO=1.05V; R8503=113K (10V220000401); Vout=FB \*(1+ (R8503 / R8502))  
 N17P-G1-->VO=1V; R8503=100K (10V220000004); VFB=0.6V; T=1.5%

# +1.8V POWER SUPPLY



# (N17)VGA\_CORE POWER SUPPLY

N16P-GX follow DG-07269

N16P-GX

N17P-G0(G1) follow DA-07933

Config A

Config B

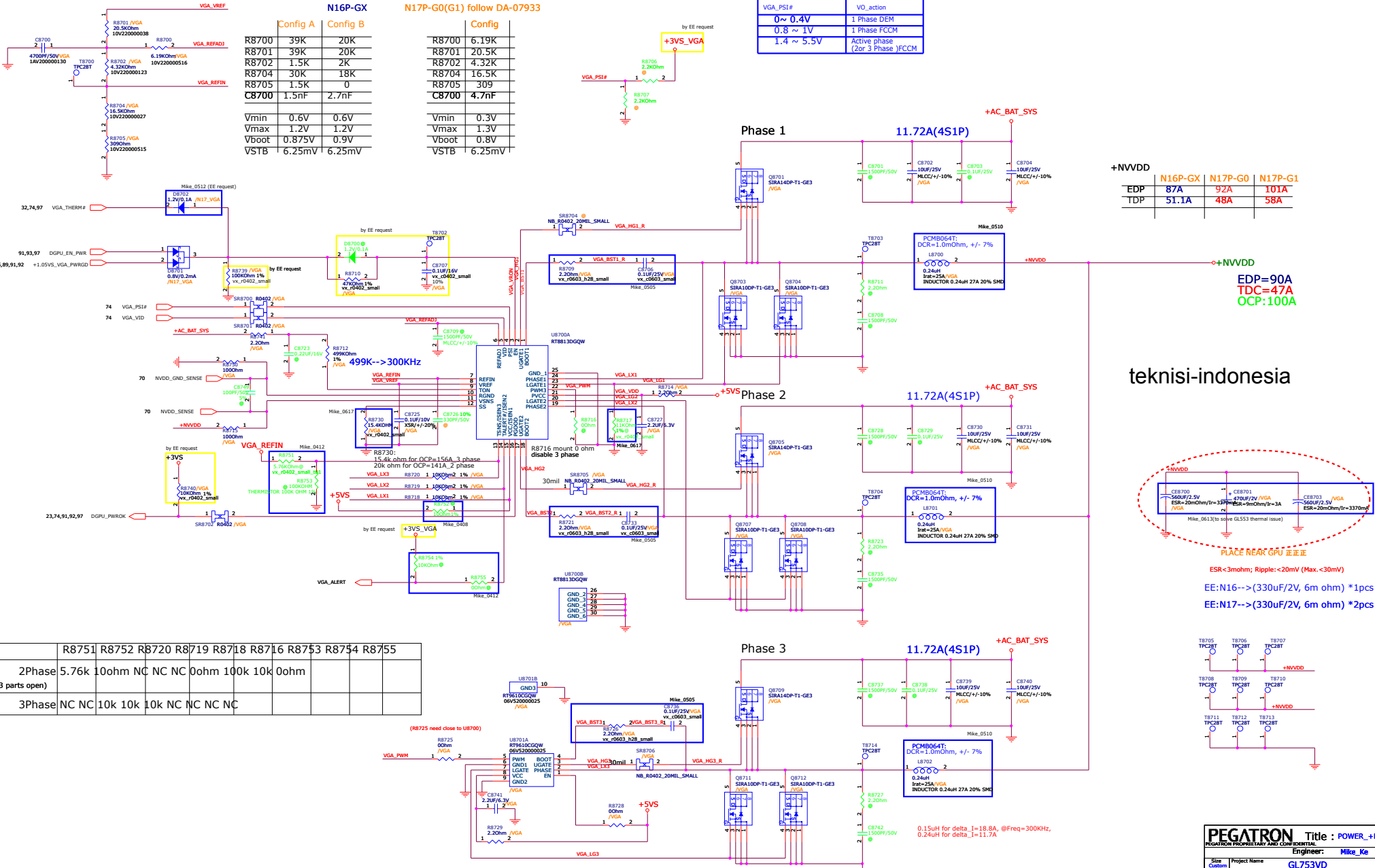
Config

R8700	39K	20K
R8701	39K	20K
R8702	1.5K	2K
R8704	30K	18K
R8705	1.5K	0
C8700	1.5nF	2.7nF

Vmin	0.6V	0.6V
Vmax	1.2V	1.2V
Vboot	0.875V	0.9V
VSTB	6.25mV	6.25mV

Vmin	0.3V
Vmax	1.3V
Vboot	0.8V
VSTB	6.25mV

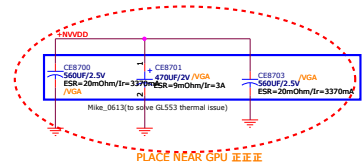
VGA_PSI#	VO_action
0 ~ 0.4V	1 Phase DEM
0.8 ~ 1V	1 Phase FCCM
1.4 ~ 5.5V	Active phase (2or 3 Phase )FCCM



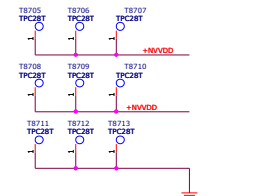
	N16P-GX	N17P-G0	N17P-G1
EDP	87A	92A	101A
TDP	51.1A	48A	58A

EDP=90A  
TDC=47A  
OCP=100A

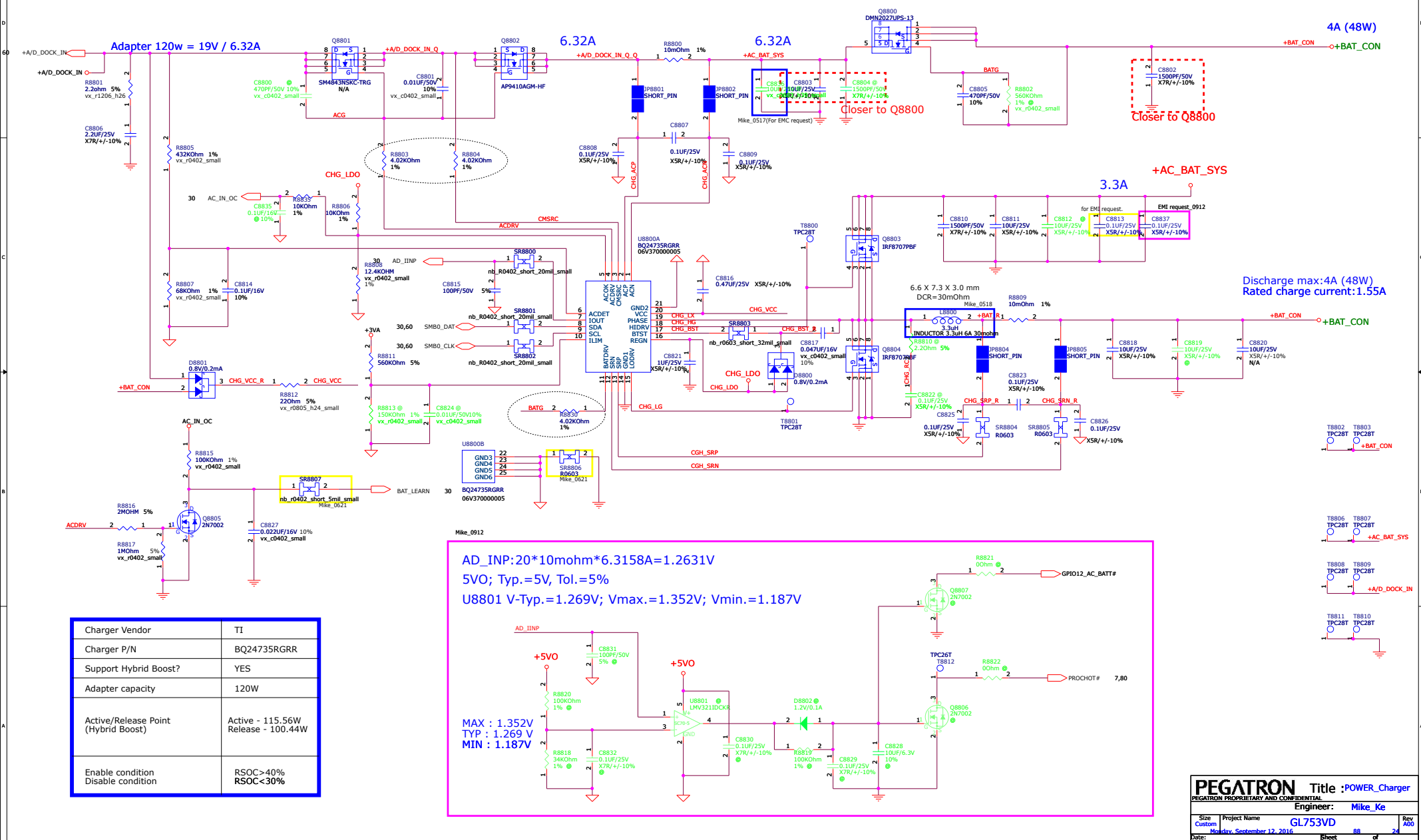
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EE: N16--> (330uF/2V, 6m ohm) \*1pcs  
EE: N17--> (330uF/2V, 6m ohm) \*2pcs



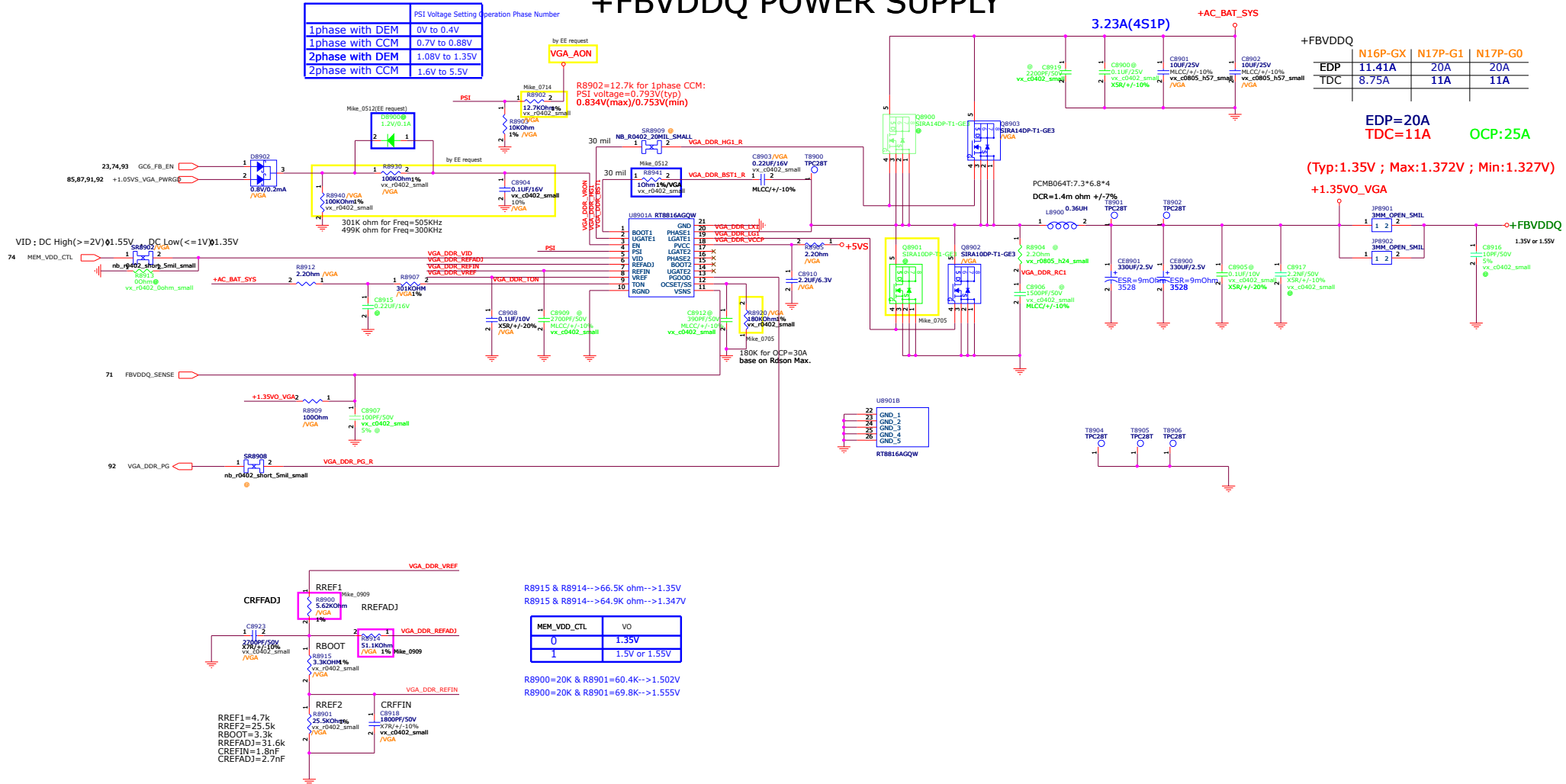
## BATTERY CHARGER



## +FBVDDQ POWER SUPPLY

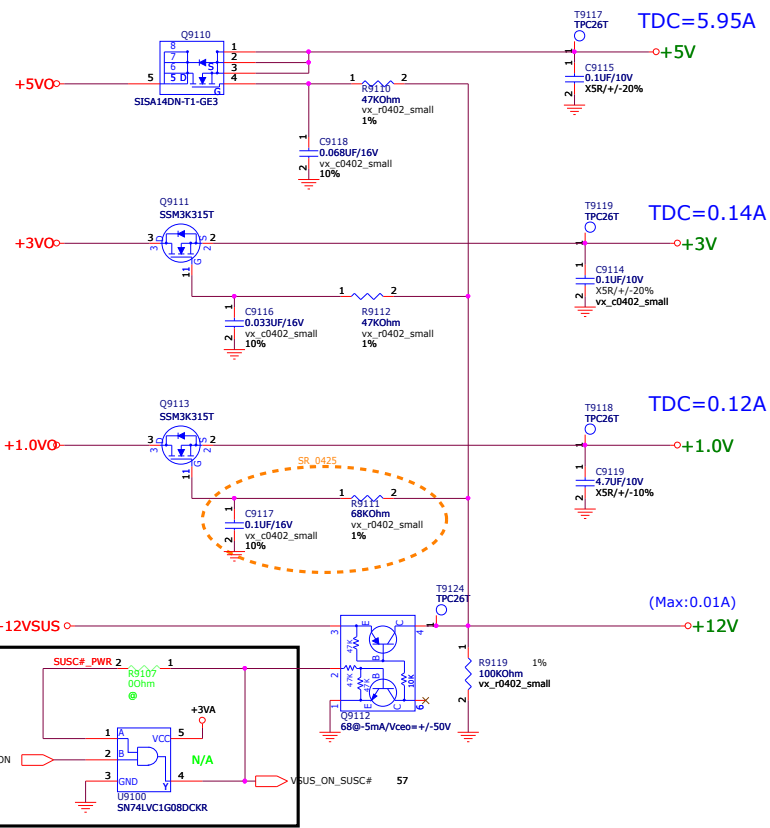
	PSI Voltage Setting	Operation Phase Number
1phase with DEM	0V to 0.4V	
1phase with CCM	0.7V to 0.88V	
2phase with DEM	1.08V to 1.35V	
2phase with CCM	1.6V to 5.5V	

R8902=12.7k for 1phase CCM:  
PSI voltage=0.793V(typ)  
0.834V(max)/0.753V(min)

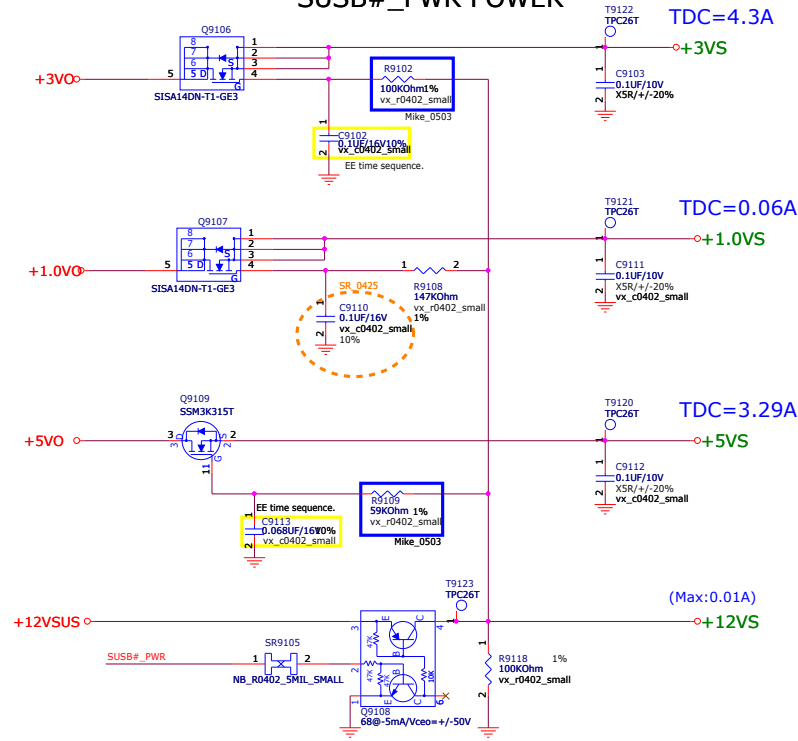


BATTERY IN DETECT

# SUSC#\_PWR POWER



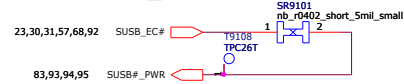
# SUSB#\_PWR POWER



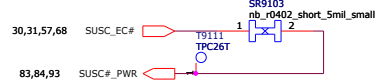
## +3VS\_VGA

	N16P-GX	N17P-G1
EDP	X	TBD
TDC	X	1A

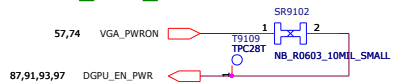
## SUSB#\_PWR POWER Control



## SUSC#\_PWR POWER Control

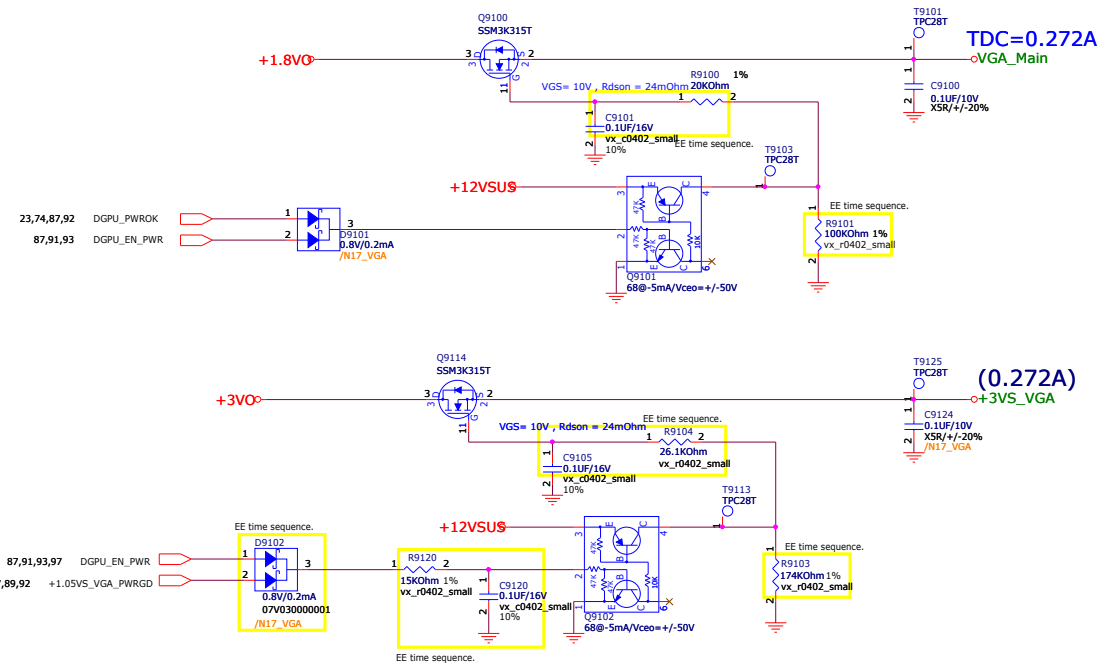


## DSC\_VGA\_PWR POWER Control



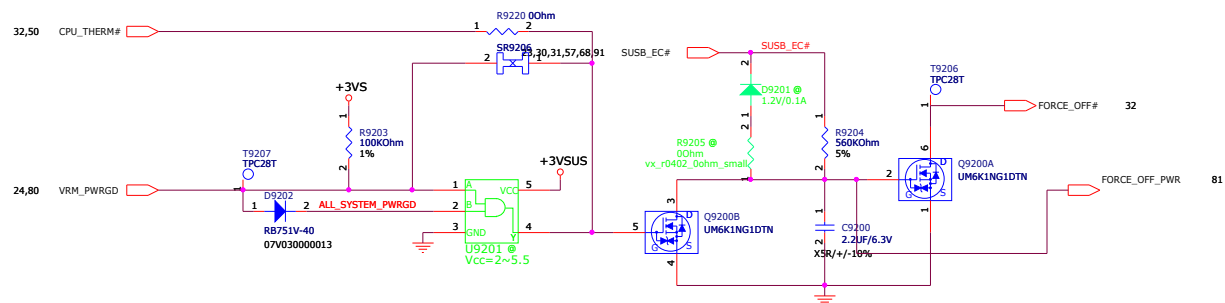
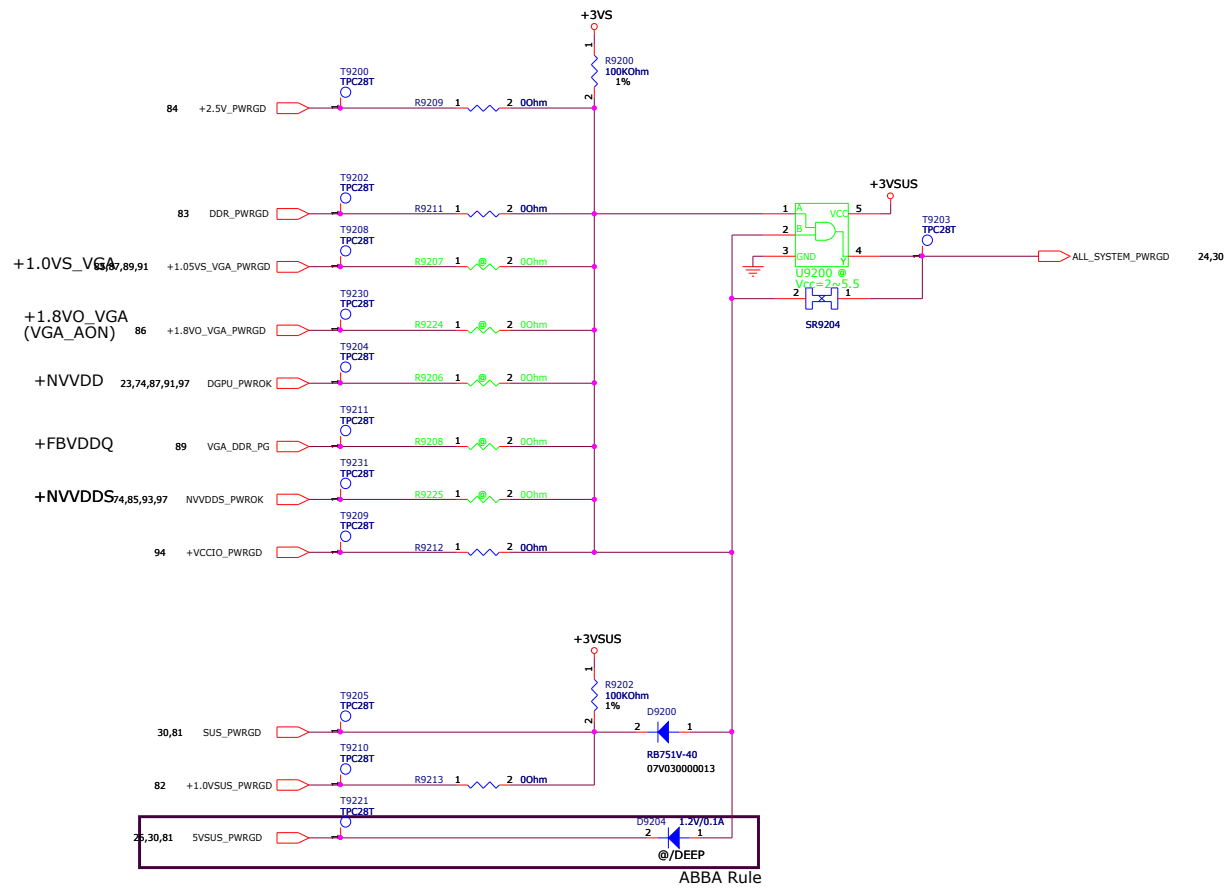
## +3VS\_VGA

	N16P-GX	N17P-G1
EDP	TBD	X
TDC	0.34A	X





## POWER GOOD DETECTOR



+AC\_BAT\_SYS → +AC\_BAT\_SYS 45,80,81,82,83,87,88,89,94,97

+BAT\_CON → +BAT\_CON 60,88

+5VA → +5VA 81

+3VA → +3VA 25,30,31,57,66,74,81,88,91

+5VO → +5VO 81,82,83,84,85,88,91,94,95

+3VO → +3VO 81,86,91,95

+1.5VO → +1.5VO 95

+5VSUS → +5VSUS 26,31,51,56,81

+3VSUS → +3VSUS 7,21,23,24,26,28,30,31,33,36,44,68,74,81,92,97

+3V → +3V 24,45,53,57,66,68,91

+5VS → +5VS 31,36,46,48,50,51,56,57,80,87,89,91,97

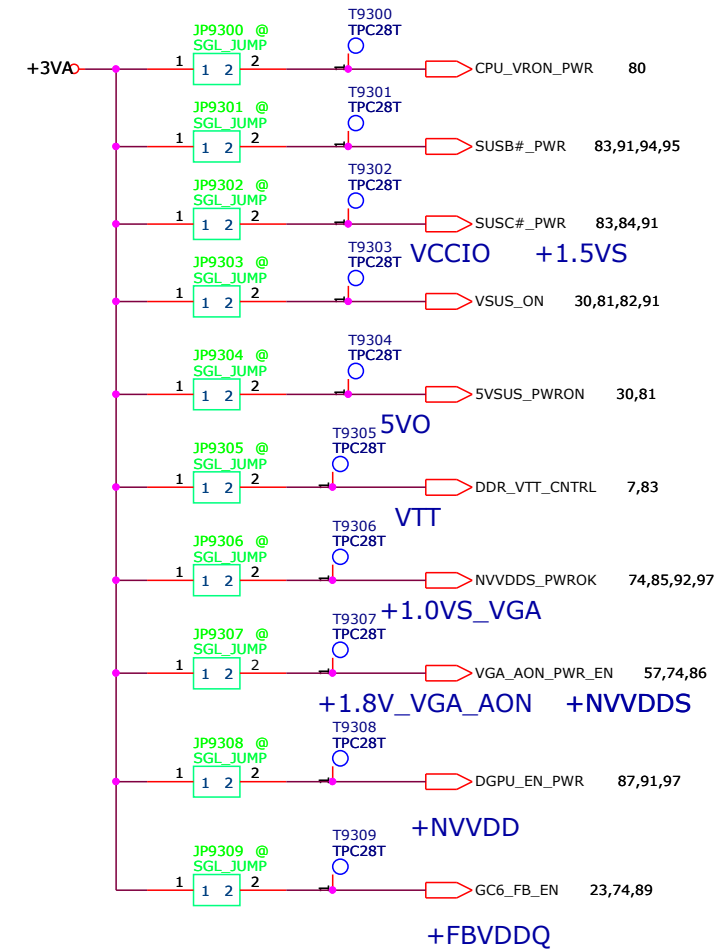
+3VS → +3VS 7,16,21,22,23,24,26,28,30,31,32,33,36,40,44,45,46,48,49,50,51,53,56,57,85,87,91,92,97

+1.5VS → +1.5VS 36,95

+VCORE → +VCORE 9,80

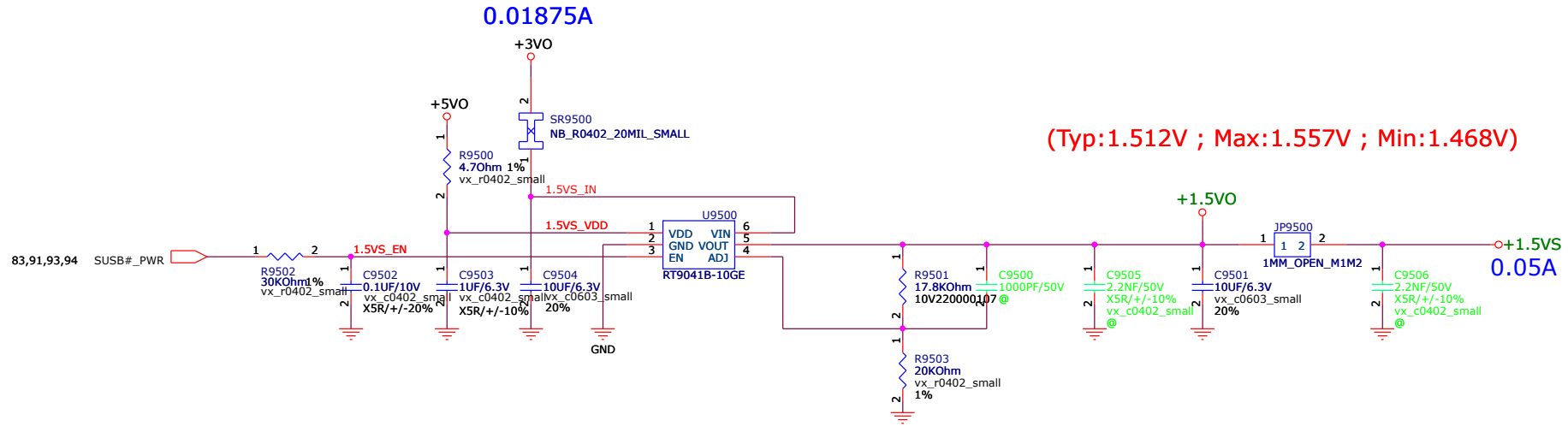
+VCCIO → +VCCIO 3,6,7,10,94

## FOR POWER TEST





# 1.5V POWER SUPPLY



$$V_{out} = V_{ref} * ( 1 + ( R1 / R2 ) )$$

Vref=0.8V +- 2%



# +NVVDDS POWER SUPPLY

N17P-G0(G1) follow DA-07933

Config	
R9723	6.19K
R9721	20.5K
R9716	4.32K
R9713	16.5K
R9741	309
C9720	4.7nF
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V
VSTB	6.25mV

	PSI Voltage Setting	Operation Phase Number
1phase with DEM	0V to 0.4V	
1phase with CCM	0.7V to 0.88V	
2phase with DEM	1.08V to 1.35V	
2phase with CCM	1.6V to 5.5V	

+NVVDDS

	N16P-GX	N17P-G0	N17P-G1
EDP	X	16A	18A
TDC	X	12A	13A

OCP:50A

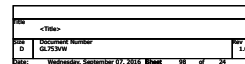
EDP=42A  
TDC=19A

EE:N17-->(330uF/2V, 6m ohm) \*1pcs  
POWER:N17-->(560uF/2.5V, 20m ohm) \*2pcs

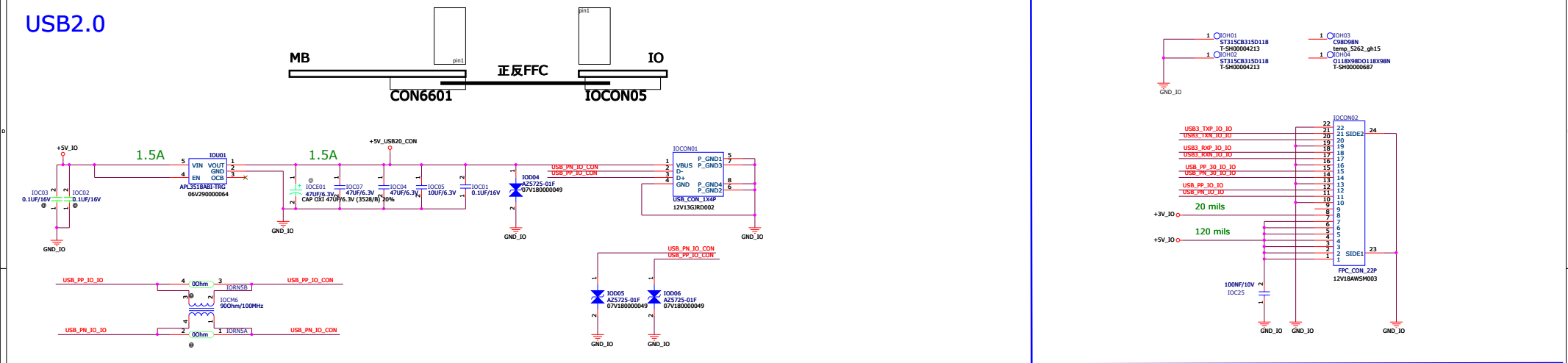
Total :ESR=3.7 mohm

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1 → 20

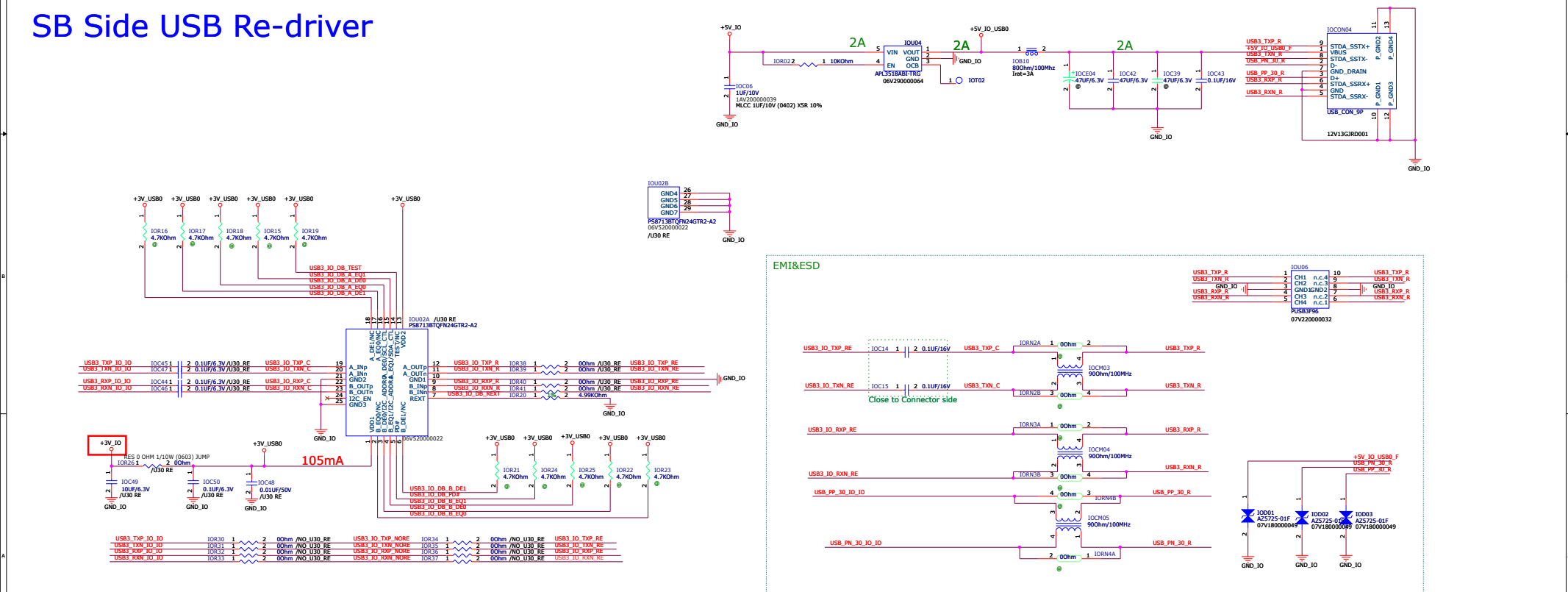


## USB2.0



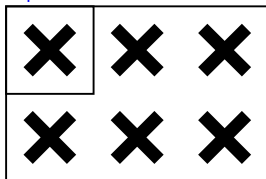
## USB3.0

## SB Side USB Re-driver



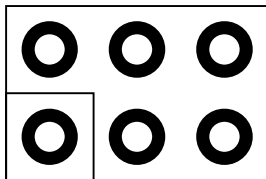
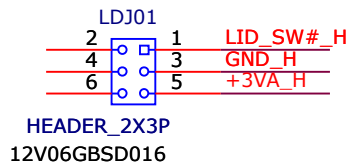


pin1\_DB  
Top view

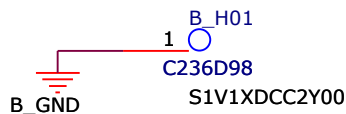


LDJ01  
pin1:LID\_SW#\_H  
pin3:GND\_H  
pin5:+3VA\_H

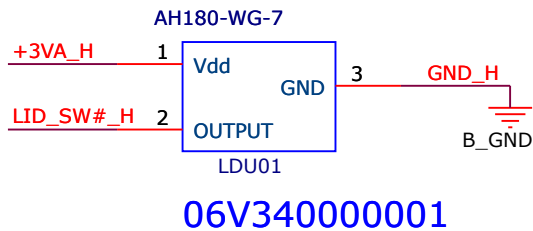
CON6602  
pin2:LID\_SW#  
pin4:GND  
pin6:+3VA



pin1\_MB  
Top view



# LID Switch



<b>PEGATRON</b>		Title : Power SW Board
PEGATRON PROPRIETARY AND CONFIDENTIAL		Engineer: Daniel Szu
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-RD Sec.3		
Size A	Project Name GL553VW	Rev 1.1
Date: Wednesday, September 07, 2016	Sheet 101 of 99	

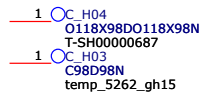
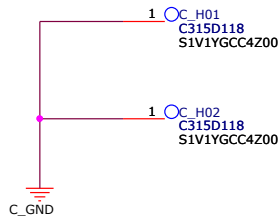
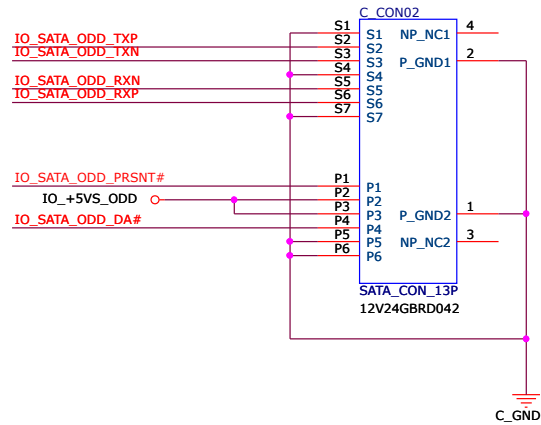
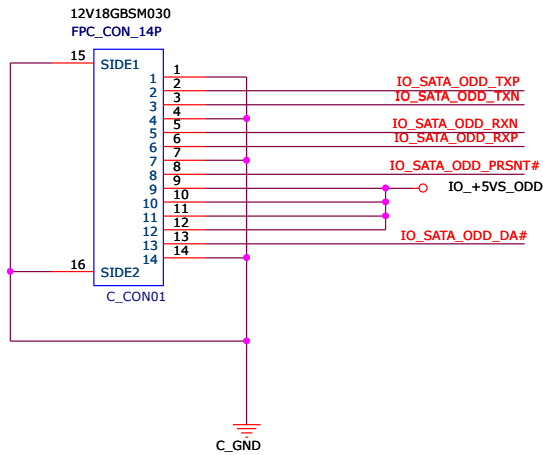


Table 5 – Standard SATA connector (3.5 inch & 2.5 inch HDD)

	Name	Type	Description	Cable Usage <sup>a,b</sup>	Backplane Usage <sup>c</sup>
Signal Segment	Signal Segment Key				
	S1	GND	Ground	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	S2	A+	Differential Signal Pair A	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	S3	A-	Differential Signal Pair A	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	S4	GND	Ground	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	S5	B-	Differential Signal Pair B	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	S6	B+	Differential Signal Pair B	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	S7	GND	Ground	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
Signal Segment "L"					
Central Connector Gap <sup>d</sup>					
Power Segment	Power Segment "L"				
	P1	Retired <sup>e,f</sup>		2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P2	Retired <sup>e,f</sup>		2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P3	DEVSLP <sup>g</sup>	Enter/Exit DevSleep	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P4	GND	Ground	1 <sup>st</sup> Mate	1 <sup>st</sup> Mate
	P5	GND	Ground	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P6	GND	Ground	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P7	V <sub>s</sub>	5 V Power, Pre-charge	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P8	V <sub>s</sub>	5 V Power	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P9	V <sub>s</sub>	5 V Power	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P10	GND	Ground	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P11	DAS/DSS/DHU	Device Activity Signal / Disable Staggered Spinup / Direct Head Unload / Vendor Specific <sup>h</sup>	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P12	GND	Ground	1 <sup>st</sup> Mate	1 <sup>st</sup> Mate
	P13	V <sub>12</sub>	12 V Power, Pre-charge	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P14	V <sub>12</sub>	12 V Power	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P15	V <sub>12</sub>	12 V Power	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
Power Segment Key					
<sup>a</sup> For specific optional usage of pin P11 (see 6.13). <sup>b</sup> Although the mate order is shown, hot plugging is not supported if using the cable connector receptacle. <sup>c</sup> All mate sequences assume zero angular offset between connectors. <sup>d</sup> The signal segment and power segment may be separate. <sup>e</sup> Previous versions of this specification assigned 3.3 V to pins P1, P2 and P3. In addition, device plug pins P1, P2 and P3 were required to be bused together. <sup>f</sup> It is recommended to have P1 and P2 connected together for the purpose of legacy functionality. Pin P3 should be a no connect if DEVSLP is not implemented.					

Table 15 – Slimline device plug connector pin definition

	Name	Type	Description	Cable Usage <sup>a b</sup>	Backplane Usage <sup>a</sup>
Signal Segment	Refer to Table 5.				
Signal Segment "L"					
Central Connector Gap					
Power Segment "L"					
Power Segment	P1	DP	Device Present	3 <sup>rd</sup> mate	3 <sup>rd</sup> mate
	P2	+5 V <sup>a</sup>		2 <sup>nd</sup> mate	2 <sup>nd</sup> mate
	P3	+5 V <sup>a</sup>		2 <sup>nd</sup> mate	2 <sup>nd</sup> mate
	P4	MD/DA	Manufacturing Diagnostic/Device Attention <sup>c</sup>	2 <sup>nd</sup> mate	2 <sup>nd</sup> mate
	P5	Gnd <sup>a</sup>	Ground	1 <sup>st</sup> mate	1 <sup>st</sup> mate
	P6	Gnd <sup>a</sup>	Ground	1 <sup>st</sup> mate	1 <sup>st</sup> mate
Power Segment Key					
<sup>a</sup> All pins are in a single row with 1.00 mm (0.039 inch) pitch on the power segment portion.					
<sup>b</sup> Ground pins in the Serial ATA Slimline device plug power segment (connector pins P5 and P6) shall be bussed together on the Serial ATA Slimline device.					
<sup>c</sup> The connection between the Serial ATA Slimline device signal ground and power ground is vendor specific.					
<sup>d</sup> The DP and MD/DA signals shall be referenced to the power portion ground pins, P5 and P6.					
<sup>e</sup> The 5 V power delivery pins in the Serial ATA Slimline device plug power segment (connector pins P2 and P3) shall be bussed together in the Serial ATA Slimline device.					

## Skylar

ke H

VID1 : 0.9V  
VID2 : 0.6V  
VID3 : 0.3V  
Vboot : 0V  
LL=2.65mohm

Rs2 & Rpu2 Resistance circuit put in EE P7  
Rs2 & Rpu2 Resistance need to close VR controller

	Rs2	Rpu2
VIDALERT#	10 ohm	100 ohm
VIDSCLK	50 ohm	45 ohm
VIDSOUT	0 ohm	Empty

